Overview

- Building behavioral models in stages
- A 5^{th}-order, 1-Bit $\Sigma\Delta$ modulator
  - Noise shaping
  - Complex loop filters
  - Stability
  - Voltage scaling

Building Models in Stages

- When modeling a complex system like a 5^{th}-order $\Sigma\Delta$ modulator, model development proceeds in stages
  - Each stage builds on its predecessor
- The design goal is to detect and eliminate problems at the highest possible level of abstraction
  - Each successive stage consumes progressively more engineering time

Building Models in Stages

- Rework and reverification of early stage models because of problems found in later stages is expensive
  - Defective silicon is much more expensive (and often fatal)
- Don't launch a multistage rework cycle every time you find a single bug

Building Models in Stages

- Our ΣΔ model development proceeds in stages:
  - Stage 0 gets to the starting line
  - Stage 1 develops a practical system built with ideal subcircuits
  - Stage 2 models key subcircuit nonidealities and translates the results into real-world subcircuit performance specifications

Building Models in Stages

- Real-world model development includes a critical stage 3:
  - Adding elements to earlier stages (hopefully only stage 2) to model significant surprises found in silicon
- The previous lecture introduced much of the stage 0 $\Sigma\Delta$ model and 1-Bit quantization background
  - What other steps are needed to arrive at a successful design?

Stage 0

- Collect references
  - Important references
  - Readable references
  - Talk to veterans to find them and sort them
- Understand the readable references
  - Build a simple model of what you think you understand
  - Start building diagnostic infrastructure

Stage 0 Models

- You can't just talk about stage 0 models with veterans and look at their stage 0 simulations
  - You've got to exercise and think with the model until you can begin to explain surprises by yourself
  - Then, in stage 1, you can ask a veteran more intelligent questions
- Stage 0 model code (download code used for last lecture) is 20% modulator loop code, 80% diagnostics
  - This ratio holds for all stages of modeling

Stage 1

- In stage 1, we'll study a model for a practical $\Sigma\Delta$ modulator topology built with ideal blocks
- Stage 1 model focus
  - Signal amplitudes
  - Stability
    - Worst-case inputs
    - Unstable systems can't graduate to stage 2
  - Quantization noise shaping

Stage 1 Models

Building the infrastructure to generate worst-case inputs and analyze model responses is of critical importance in stage 1

- You must tap into your organization's technical wisdom to learn what those worst-case real world inputs are

Models can only tell you the right answers if you ask them the right questions!

ΔΣ Modulator Filter Design

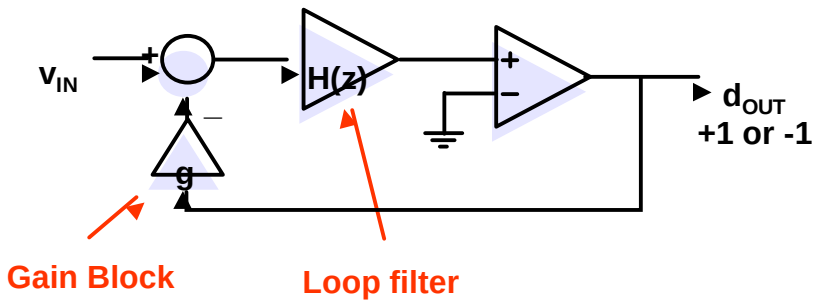
- Procedure
  - Establish requirements
  - Design noise-transfer function, NTF
  - Determine loop-filter, H
  - Synthesize filter
  - Evaluate performance, stability

Ref: R. W. Adams and R. Schreier, "Stability Theory for ΔΣ Modulators," in Delta-Sigma Data Converters, S. Norsworthy et al. (eds), IEEE Press, 1997, pp. 141-164.

Modulator Specification

- Example: Audio ADC
  - Dynamic range — DR — 16 Bits
  - Signal bandwidth — B — 20 kHz
  - Nyquist frequency — f_N — 44.1 kHz
  - Modulator order — L — 5
  - Oversampling ratio — $M = f_s/f_N$ — 64
  - Sampling frequency — f_s — 2.822 MHz
- The oversampling ratio M chosen based on
  - SQNR > 120dB (20dB below thermal noise)
  - Experience (e.g. Figure 4.14 in Adams & Schreier)

Modulator Block Diagram



Noise Transfer Function, NTF(z)

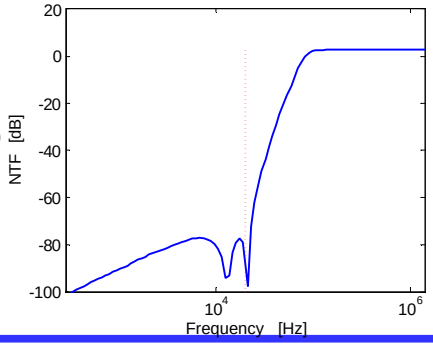
```
% stop-band attenuation ...
% reduce if design is not stable

Rstop = 80;
[b,a] = cheby2(L, Rstop, 1/M, 'high');

% normalize (for causality)
b = b/b(1);
NTF = filt(b, a, 1/fs);

% check stability (mag < 1.5)
[mag] = bode(NTF, pi*fs)

>> mag =  1.32
```

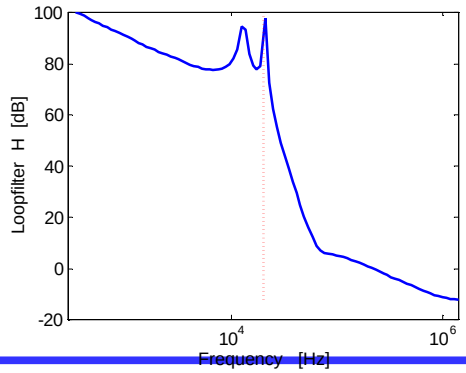


Loop-Filter, H(z)

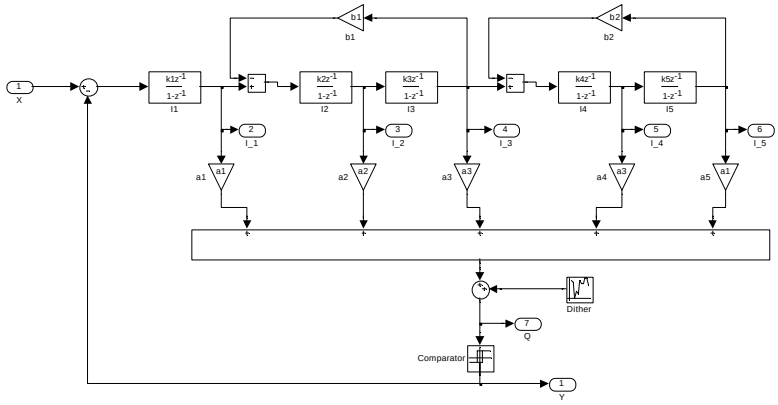
```
H = inv(NTF) - filt(1, 1, 1/fs);

% check causality … y(1) should be 0
y = impulse(H);
y = y(1)

>> y =  0
```



Filter Topology

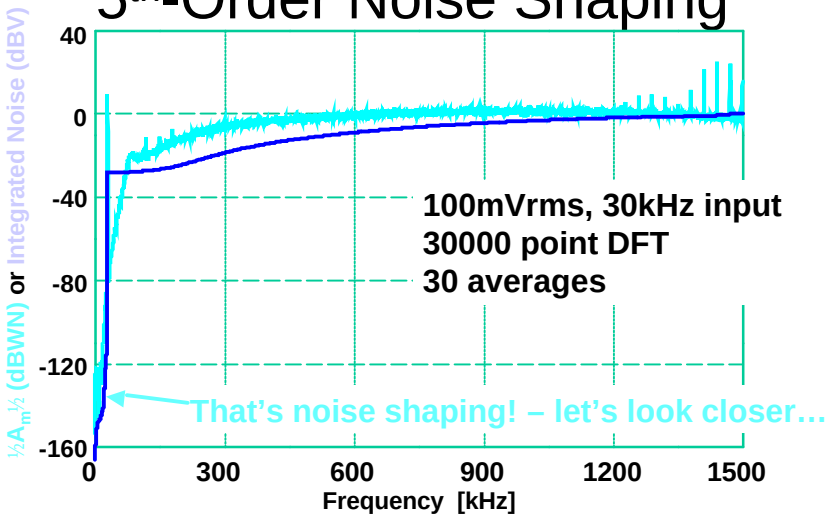


Rounded Filter Coefficients

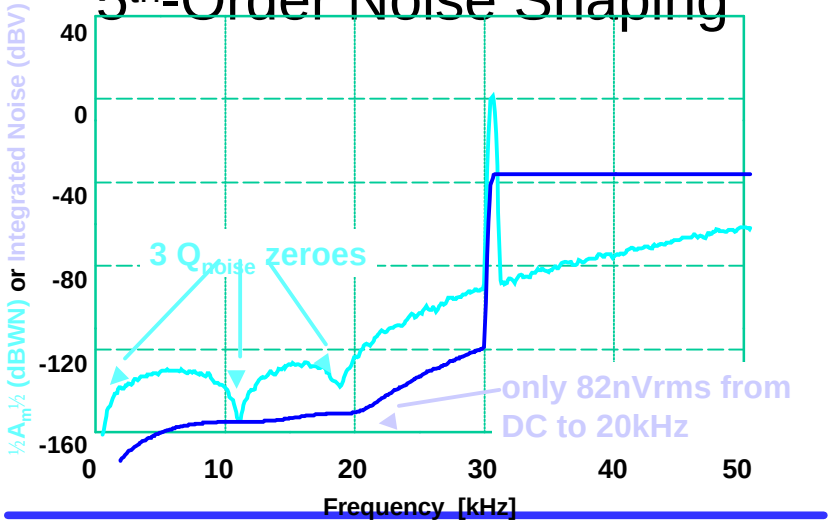
```
a1=1;          k1=1;          b1=1/1024;
a2=1/2;        k2=1;          b2=1/16-1/64;
a3=1/4;        k3=1/2;
a4=1/8;        k4=1/4;
a5=1/8;        k5=1/8;
```

Ref: Nav Sooch, Don Kerth, Eric Swanson, and Tetsuro Sugimoto, “Phase Equalization System for a Digital-to-Analog Converter Using Separate Digital and Analog Sections”, U.S. Patent 5061925, 1990, figure 3 and table 1.

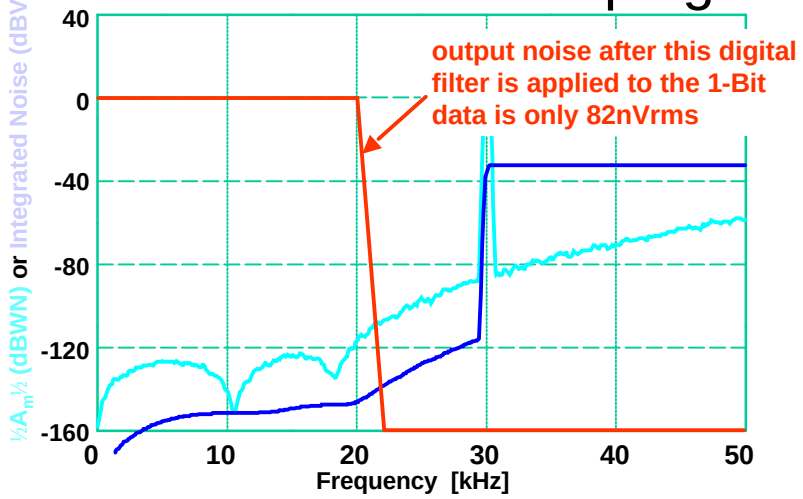
5th-Order Noise Shaping



5th-Order Noise Shaping



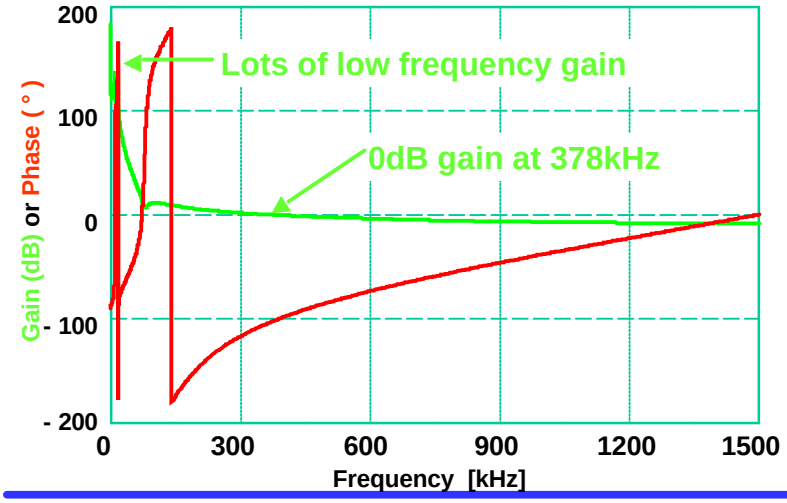
5th-Order Noise Shaping



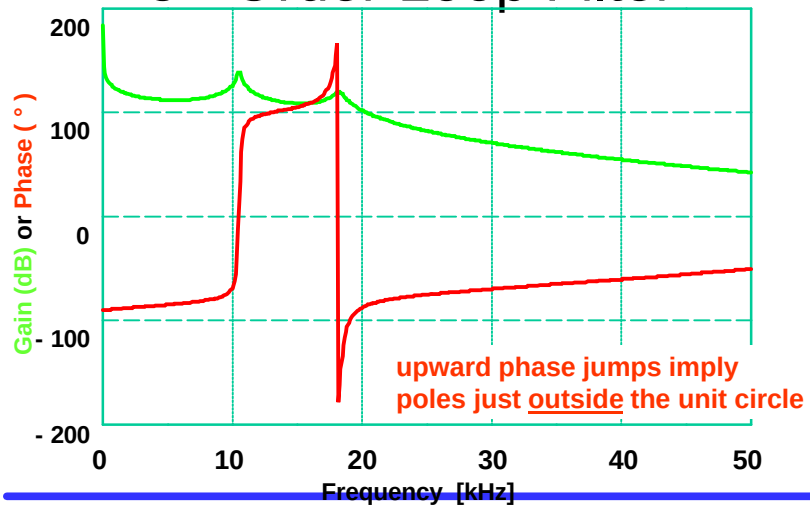
5th-Order Noise Shaping

- The 1Vrms 1-Bit quantization noise is shaped to sum to only 82nVrms in the audio band
  - That's over 140dB of dynamic range
- ΣΔ modulators are usually designed so that their quantization noise is negligible in the frequency band of interest
  - Thermal noise sources dominate
- Let's look at the loop filter transfer function…

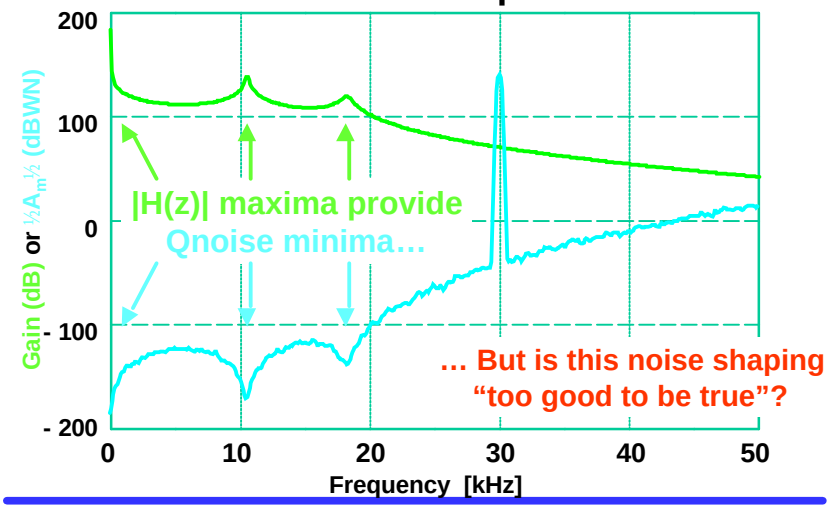
5th-Order Loop Filter



5th-Order Loop Filter



5th-Order Loop Filter

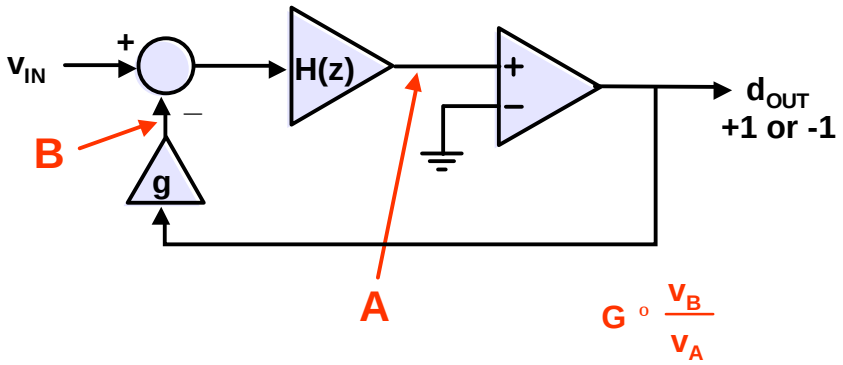


5th-Order Loop Filter

- The fact that H(z) has poles outside the unit circle doesn't mean that the entire ΣΔ modulator is unstable
  - The modulator's stability depends on its closed loop poles
- All loop variables (∫1, ∫2, ∫3, ∫4, ∫5) have the same closed loop poles
  - If one is stable, they all are

Modulator Root-Locus

The nonlinear modulator system operates at some effective gain G between points A and B:



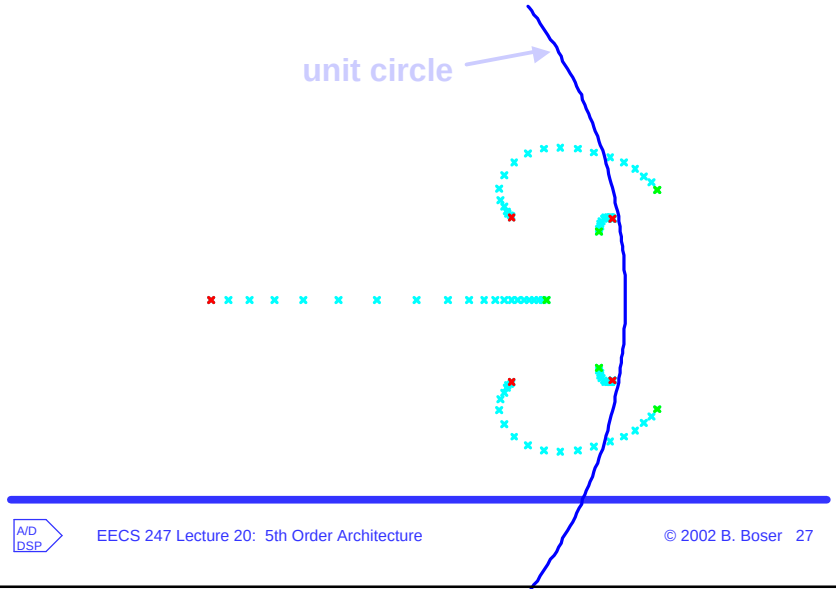
Modulator Root-Locus

- G may be a function of both v_{IN} and g
- The modulator closed loop poles are the zeroes of the function 1+HG:

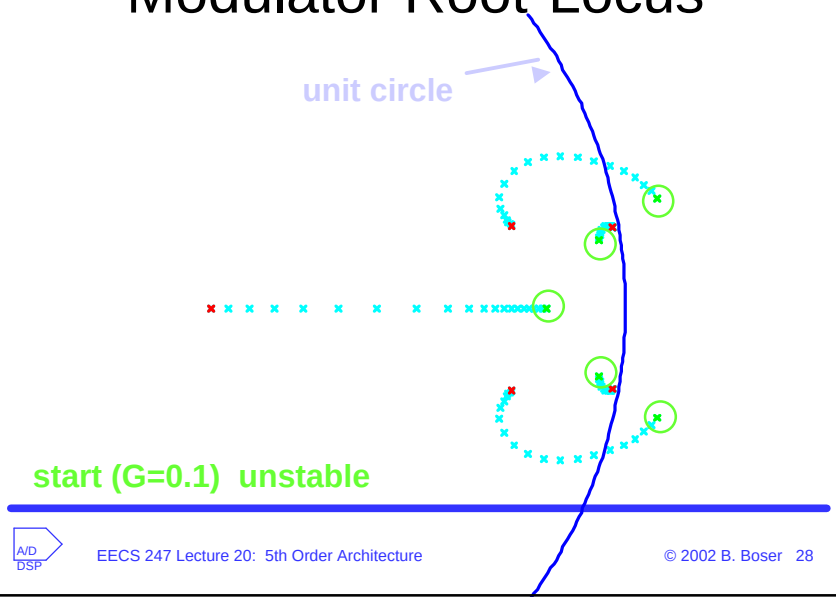
$$\frac{D_{OUT}(z)}{V_{IN}(z)} = \frac{HG/g}{1 + HG}$$

- We'll plot closed loop poles in the z-plane as G varies from 0.1 to 10 in equal log steps …

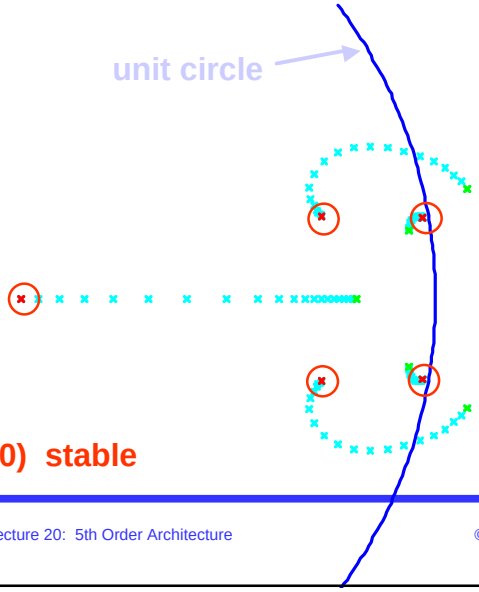
Modulator Root-Locus



Modulator Root-Locus

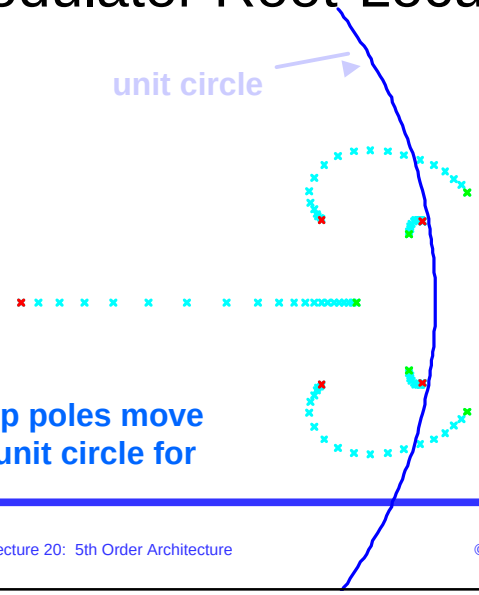


Modulator Root-Locus



stop (G=10) stable

Modulator Root-Locus

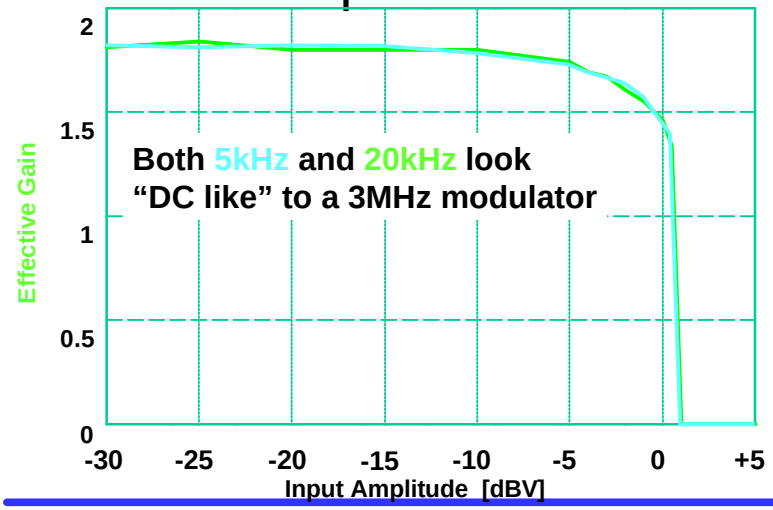


Closed-loop poles move inside the unit circle for G > 0.4

Effective Gain

- If our linearized model is valid (a big if)
  - For G > 0.4, the modulator system is stable
  - For G < 0.4, it's unstable
- Presumably, the noise shapes in slides 18 and 23 were produced by a stable system
  - We'll evaluate G for 5kHz and 20kHz sinusoidal inputs varying in amplitude from –30dBV to +5dBV…
  - While we're at it, we'll capture minimum and maximum signal levels throughout the modulator

Sinewave Input Effective Gain



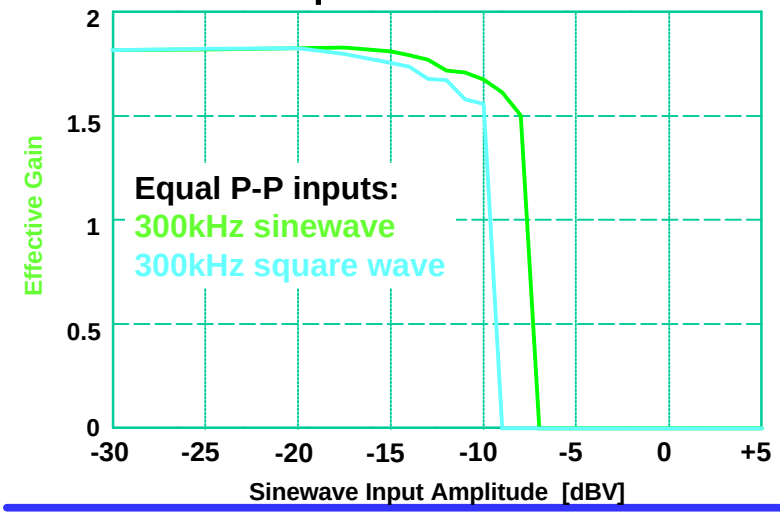
Effective Gain

- As the input amplitude increases, the signal at the quantizer input grows, and G falls
- Just over 1Vrms, G falls to below 0.4, and
  - The system becomes unstable
  - Loop variables grow without bound
    (opamps in a real analog circuit will just run up to power supply rails)
  - Noise shaping is lost

Effective Gain

- It's highly unlikely that audio sinewaves provide the worst case inputs for stability
  - To evaluate any model, you've got to know what the worst case inputs are
- Let's look at inputs that aren't "dc-like" and aren't sinusoidal (square waves)…

300kHz Input Effective Gain



Modulator Stability

- The sensitivity of ΣΔ modulators to high frequency square wave inputs was first discovered on breadboards
  - No one thought to provide such inputs to early modulator simulations
- Worst-case square wave frequencies are roughly equal to the frequency of the highest Q pole in the noise shape
  - A key job of the antialiasing filters used in front of ΣΔ modulators is to reduce out-of-band signals to safe levels

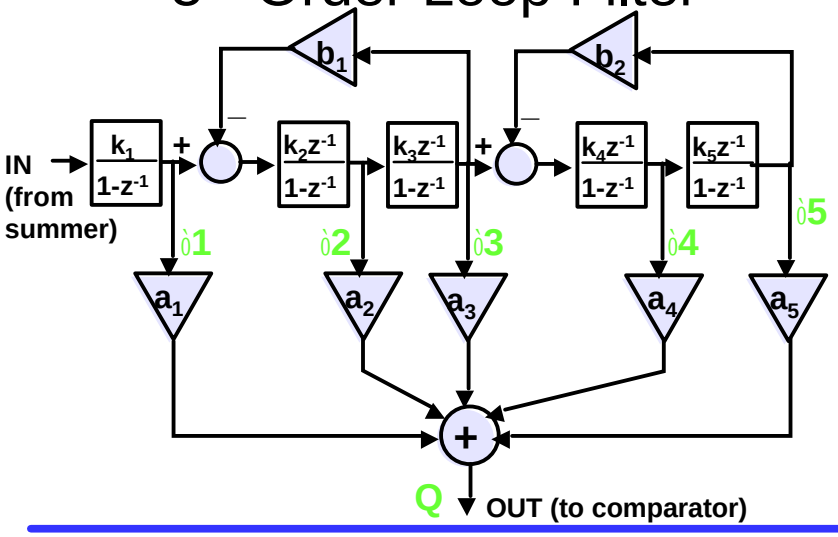
Modulator Stability

- 5000 point simulations such as those in the previous slides don't guarantee stability
  - Sometimes millions of time points are required before an unstable modulator blows up
  - When it explodes, G falls very quickly
- Square wave tolerance is a fast, effective basis for comparing the relative stability of different modulator topologies

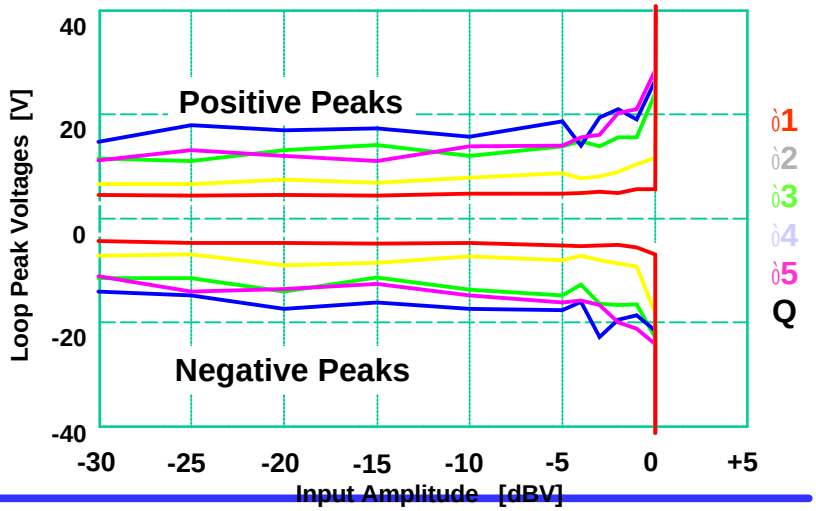
Voltage Scaling

- Given that the modulator is stable for 1Vrms inputs, let's move on to look at the state variable voltages under various input conditions
  - Loop state variables and the filter output are labeled green on the next slide
- Peak signal levels and signal standard deviations are easy to obtain in MATLAB
  - We'll examine voltages for a 5kHz sinusoidal input …

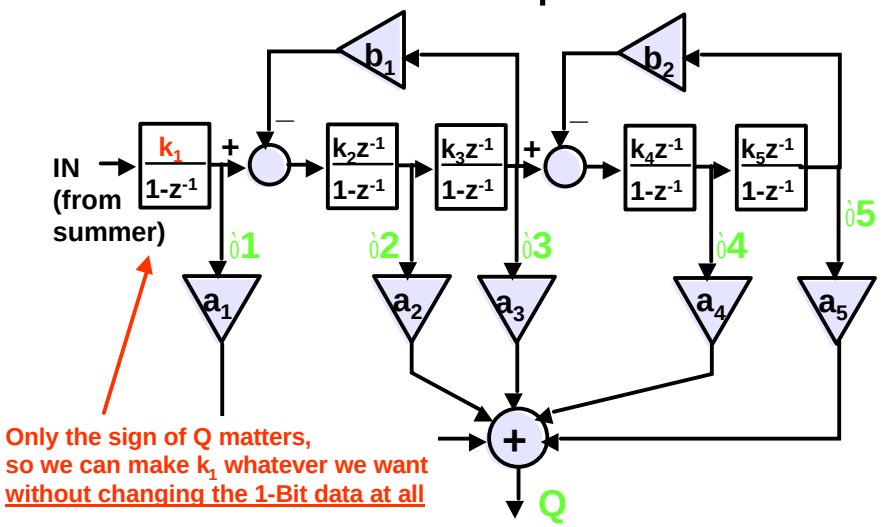
5th-Order Loop Filter



5kHz Input Loop Voltages



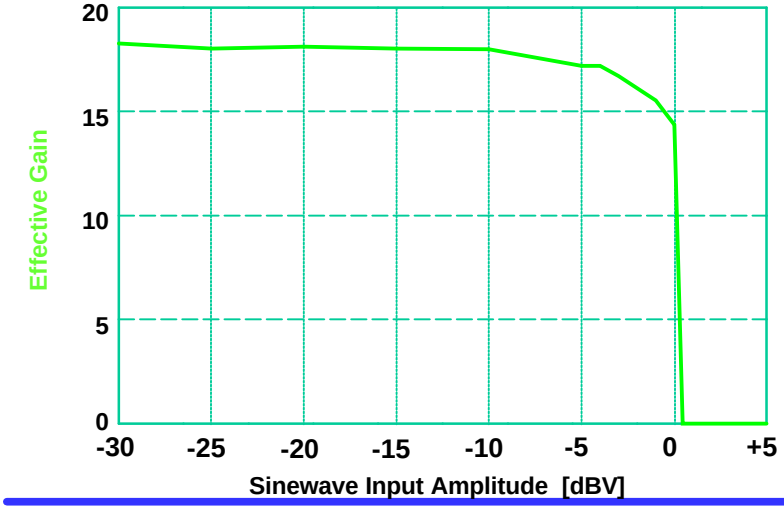
5th-Order Loop Filter



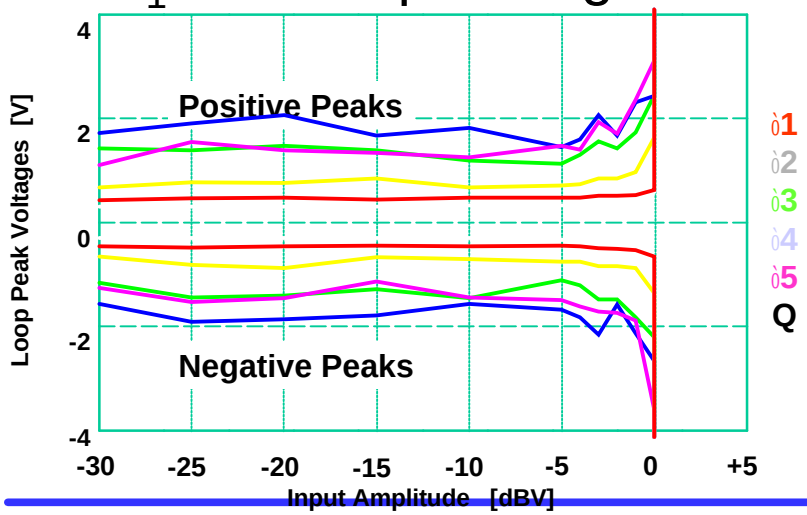
5kHz Input Loop Voltages

- If we scale k_1 by 0.1,
  - All state variables and Q scale by 0.1
  - But since the comparator output is fixed, G increases 10X
- The change in k_1 doesn't change the shape of the root locus, either
  - The effective gain for each root position is increased 10X
  - G > 4 is now required for stability

5kHz, k_1=0.1 Effective Gain



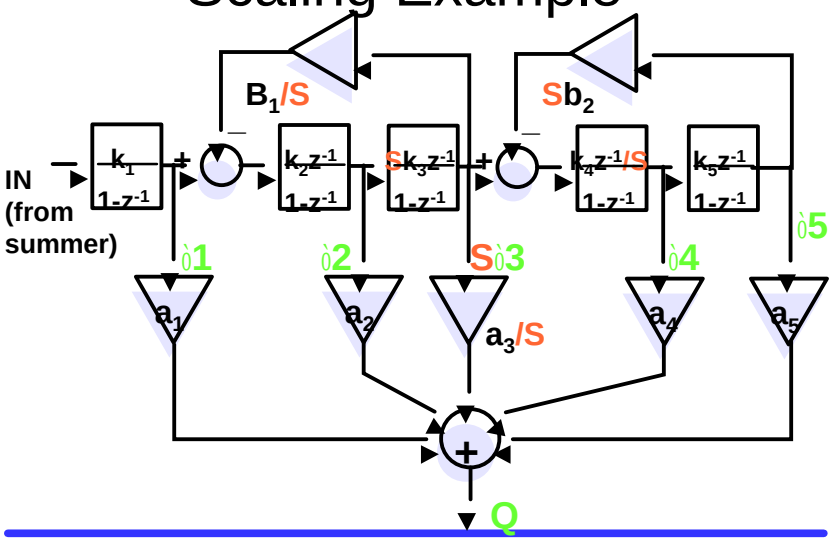
k_1=0.1 Loop Voltages



Loop Voltage Scaling

- Before we scale k_1 down any lower, we note that ∫3, ∫4, and ∫5 have substantially larger swings than ∫1 and ∫2
- Just about any filter topology allows scaling tricks which change internal state variable amplitudes without changing the filter output
  - The next slide shows an example

Scaling Example



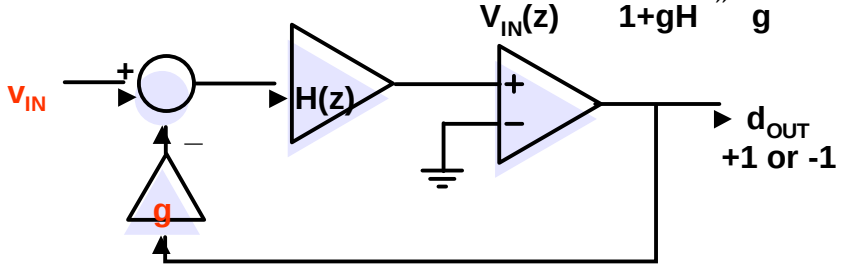
Input Range Scaling

- Slides 40 and 44 indicate inadequate stability margins for 1Vrms sinewave inputs
- Scaling the DAC output levels adjusts the modulator input range
  - If V_{IN} and the DAC outputs are scaled up by the same factor g, the 1-Bit data is completely unchanged
  - Of course, increasing the range also increases the quantization noise … the dynamic range and peak SQNR stay the same!
  - If the DAC output levels are increased and the analog full scale is held constant, the stability margin improves … at the expense of reduced SQNR

Input Range Scaling

Increasing the DAC levels by g reduces the analog to digital conversion gain:

$$\frac{D_{OUT}(z)}{V_{IN}(z)} = \frac{H}{1+gH} \approx \frac{1}{g}$$

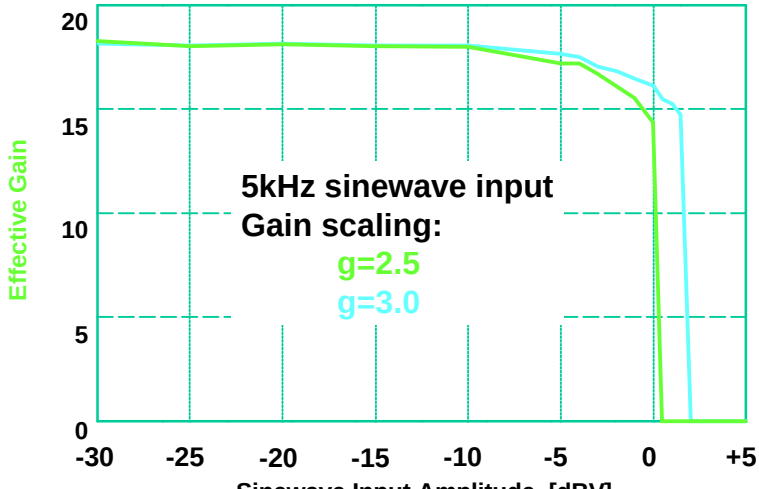


increasing v_{IN}, g by the same factor leaves 1-Bit data unchanged

Stage 1 Modulator

- We'll increase g from 2.5 to 3.0 to provide a 2dB increase in stability margin for a 1Vrms full scale input
- We'll also implement the loop voltage scaling changes suggested in slide 45
- The result is our first-pass stage 1 modulator, and its performance appears on the following slides …

Modulator Effective Gain



Loop Voltages