UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

	Project	**IC776CA**
B. E. BOSER	**Due Tue, Dec 5, 2006**	**Fall 2006**

Reference

[1] Chi-Hung Lin, K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm^2," IEEE J. Solid-State Circuits, Vol.33, pp. 1948-1958, Dec 1998.

Objective

The above referenced DAC was optimized for best performance in a particular technology. You are to carry out an architecture level re-design and yield analysis for this DAC given a new set of technology parameters and performance objectives.

The general architecture of the DAC under consideration is fixed and identical to that in [1]. The design variables to be optimized are: (1) bit segmentation (2) area of the unit elements. These variables should be chosen to minimize the DAC area while meeting the given linearity specifications at the desired yield.

The goal is to gain experience in using a result form the literature and analyzing and simulating a mixed analog design.

Design and Technology Parameters

Parameter	Description	Value
A_{unit}	Area of unit current source	Optimize
k_ε	Unit element Matching parameter	3%μm
σ_ε	Standard deviation of unit element mismatch	$k_\varepsilon/sqrt(A_{unit})$
M	Number of bits in segmented MSB section	Optimize
A_{decode}	Approximate decoder and routing area	$2^M \cdot 400\mu m^2$

Target Specifications

Parameter	Description	Value
B	Resolution	10 bits
INL_{spec}	Worst case integral nonlinearity	< 0.4 LSB
DNL_{spec}	Worst case differential nonlinearity	< 0.1 LSB
Y	Yield (applies to "worst case" DNL and INL codes)	99.73%
A_{total}	Total unit element and decoder area	$2^B \cdot A_{unit} + A_{decode}$ **(Minimize)**

Deliverables

You are to submit a concise project report that documents your design procedure and obtained results. Your report should be formatted ***exactly*** as indicated below (additional pages will not be considered):

(1) (1…3 pages): Hand calculations and analysis that leads to the chosen segmentation and unit element area. Include a plot similar to Fig. 9 of [1] to illustrate your chosen "optimal point". In this diagram, plot the DAC area in μm^2 (log scale) versus the design parameter M (linear scale in bits).

(2) (2 Pages): Envelope and RMS plots of the converter's DNL and INL (Fig. 7 and Fig. 8 of [1]) for 100 statistical runs. Annotate both plots with the given worst-case DNL and INL specification bounds as horizontal lines. Also mark your simulated worst-case standard deviation $\sigma_{DNL,}$ and σ_{INL} on the RMS plot.

(3) (1 Page): Performance summary table (see attached).

Appendix (No page limit): Code used for yield simulation.

Submit your report as a pdf or Word document to huifangq@eecs.berkeley.edu

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Name:

Result Summary

Parameter	Description	Analysis	Simulation
M	Number of bits in segmented MSB section		
A_{unit}	Area of unit current source [μm^2]		
A_{total}	Total unit element and decoder area [μm^2]		
σ_{INL}	Max. INL standard deviation [LSB]		
σ_{DNL}	Max. DNL standard deviation [LSB]		
INL_{spec} /σ_{INL}	INL confidence interval		
DNL_{spec} /σ_{DNL}	INL confidence interval		