**UNIVERSITY OF CALIFORNIA**

**College of Engineering**

**NTU 776CA (EECS 247)**

**Final (180 minutes)**

**December 9-13, 2002**

Exam is open-book, open-notes. Clearly mark results with box around. No credit for ambiguous solutions. Show derivations. Return this cover page. Good luck!

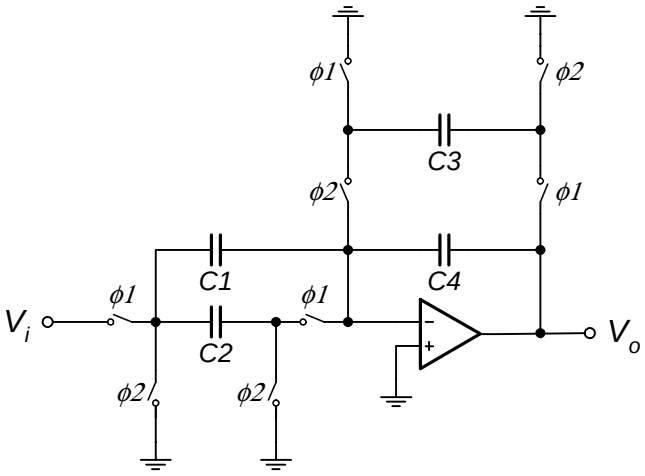
**Name:**_____

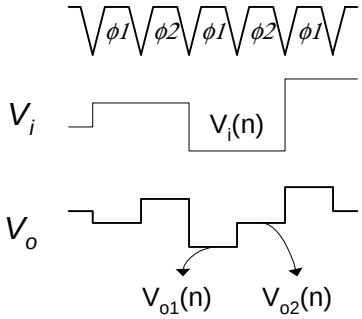
| PROBLEM | SCORE |
|---|---|
| 1 | |
| 2 | |
| 3 | |
| **Total** | |

1. [40] Derive the Z-domain voltage transfer function *H(z)* of the following switched-capacitor filter for both phases $\phi 1$ and $\phi 2$. You may assume the op amp is ideal with infinite gain and bandwidth. *Vin* updates in $\phi 2$ and holds in $\phi 1$. *Vout* changes during both $\phi 1$ and $\phi 2$.

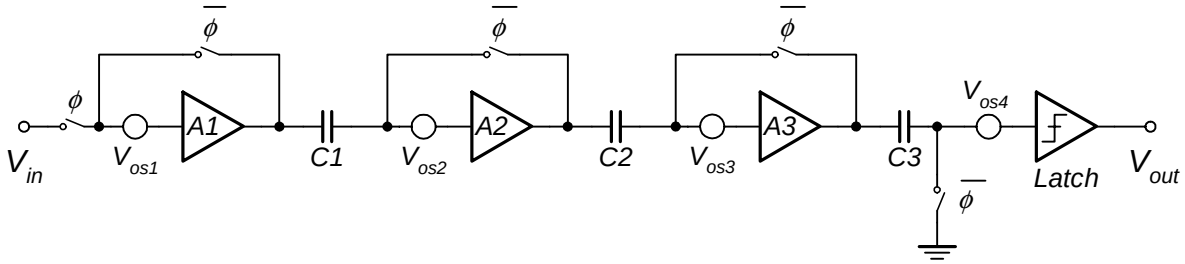
a) Derive $H_1(z)$= *Vout/Vin* during phase $\phi 1$. [20]

b) Derive $H_2(z)$= *Vout/Vin* during phase $\phi 2$. [20]



2. [20] In flash A/D converters, multi-stage preamp topology is usually adopted to reduce the comparator offset. In the following diagram, a three-stage cascaded inverter chain is used as the preamp. Assume *A1 = A2 = A3 = -4* and each inverter has an input referred offset voltage *Vosi*. The comparator (latch) has an offset of *Vos4*. The inverters are auto-zeroed (input and output shorted before comparison is performed) to reduce the offsets of themselves. You may assume all switches are ideal.

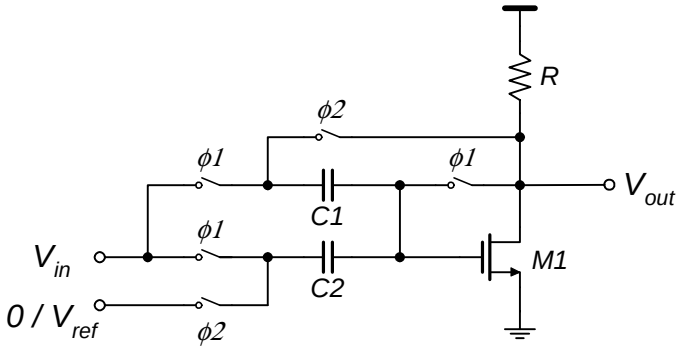



a) Explain the functionality of capacitors *C1* through *C3*. [5]

b) Derive an expression for the total input-referred offset voltage due to all preamps and the latch. [10]

c) If all offset voltages are roughly the same, which stage, in your opinion, contributes the most of the overall input-referred offset? Could you suggest a simple auto-zeroing circuit that further reduces this dominant offset error? [5]

3. [40] The following circuit diagram shows a fast residue amplifier designed for digitally corrected 1-b/stage pipelined A/D converters. A single transistor amplifier exhibits very high speed, but suffers from finite DC gain effect and nonlinearity. Assume capacitors are perfectly matched (*C1 = C2 = C*). Input voltage is sampled in phase $\phi 1$ (note that the sampling operation also performs auto-zeroing) and amplified in phase $\phi 2$. In $\phi 2$, *C2* is connected to either *0* or *Vref* depends on the *Vin* value. If *Vin* is below *Vref/2* (comparator decision *D = 0*), then *C2* is connected to *0*; if it is above *Vref/2* (comparator decision *D = 1*), then *Vref*. Ignore all parasitics. Assuming the digital correction algorithm is not applied, answer the following questions:




a) If the open-loop gain of the amplifier formed by *M1* and *R* is *-A*, derive a closed-form expression for the output residue voltage *Vout* in terms of *Vin*, *Vref*, and comparator decision *D* (you may assume *Vgs* of *M1* is 1V when $\phi 1$ is closed). [20]

*Hint: Note the quiescent biasing point of the amplifier is that when $\phi 1$ is closed. The open-loop gain is defined in terms of the signal swing where quiescent biasing is removed.*

b) Suppose we use this residue amplifier in the 1st stage of a 10-bit pipelined A/D converter. If *A = 40* is constant, how many missing codes are there around *Vref/2* (assuming the following 9-bit converter is ideal and is designed to resolve out of range signals)? [20]