UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences
NTU IC-776CA

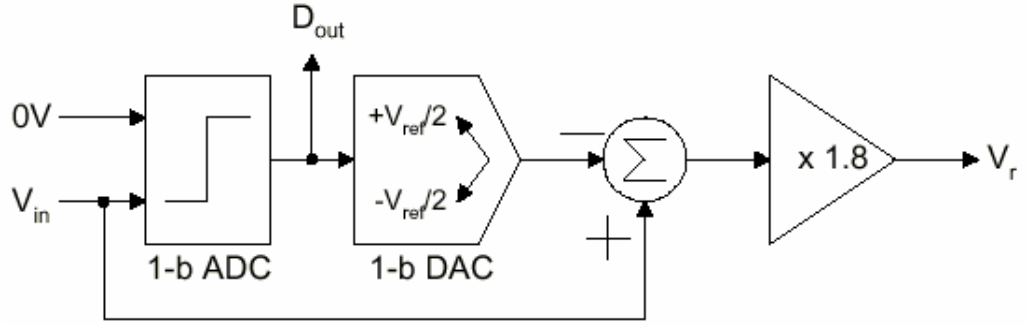
Homework 5 **EECS 247**
B. E. BOSER **Due Thursday, November 17, 2005** **Fall 2005**

1. Consider a 6-bit flash ADC with an ideal reference resistor string and V_{ref} = 1V. Assume that the comparators have an offset voltage with standard deviation σ_{os} = 3mV. What are the standard deviations of the converterís worst case DNL and INL?

2. A 16-bit pipeline ADC is implemented with 1-bit stages (just one comparator per stage). What is the maximum interstage gain for which a ±0.1 V_{ref} comparator offset can be tolerated? How many stages are required to get 16-bit resolution? (Converter voltage range ±V_{ref})

   Hint: To simplify things, design each stage to produce a residue that *never leaves the box* for up to ±0.1V_{ref} comparator offset.

3. The figure below shows one stage of a pipelined ADC. (Converter voltage range ±V_{ref})
   a) Plot V_r as a function of V_{in} / V_{ref}.
   b) What is the maximum comparator offset relative to V_{ref} that can be accommodated with digital error correction? Assume everything else is ideal.



4. Shown below is the schematic of an NMOS sampler used in the front-end of a B-bit ADC. The RC time constant of this circuit was chosen such that it settles to within 1 LSB in one half-clock period. R is the equivalent resistance of the switch. Derive an expression for the input referred total thermal noise of the sampler in terms of R, B, fs, the Boltzmann constant and temperature.