UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences
NTU IC-776CA

	Homework 4	**EECS 247**
B. E. BOSER	**Due Thursday, November 10, 2005**	**Fall 2005**

1. Your friend at Stanford just got his 12-bit prototype ADC back from the fab and tells you about his measurement results:
  - The SQNR seems to be excellent, at least 76dB
  - For one of his chips, the DNL does not look so great, he measured DNL=+0.1/-1.8 LSB.
  - On another chip, the measured INL is 0.6LSB, so he concludes that this particular converter is not monotonic.
  - Finally, he found a third chip that looks great: DNL=+0.4/-0.4 LSB, and INL=+0.1/-0.1 LSB

What is wrong with the above statements? Explain briefly.

2. The graph below shows a histogram of the output codes obtained for a 4-bit ADC with a linear ramp input. Calculate the peak positive and negative DNL and INL in LSBs.
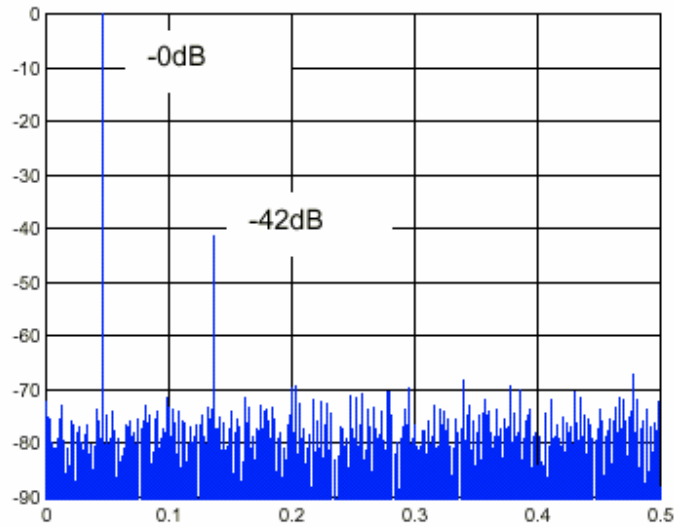
3. Shown below is a 4096-point FFT of the output of an A/D converter for full-scale sinusoidal input. Estimate the INL of the converter in LSBs.

Note 1: *the definition of INL requires that the offset and gain of the ADC are adjusted for zero error at the end points (full scale).*

Note 2: $\sin^3 \alpha = \dfrac{3}{4}\sin \alpha - \dfrac{1}{4}\sin 3\alpha$

4. An R-string DAC is fabricated with resistors with $\sigma_{\Delta R/R}$=0.2%. For the INL and DNL to be better than 0.5 LSB,
   a) What is the expected yield of a 12-bit DAC?
   b) What is the maximum achievable resolution (no trimming or calibration), if a yield of 99% good parts is desired?

5. Consider a resistor string DAC with a deterministic, linear error gradient as illustrated below. The jth resistor in the ladder deviates from its ideal value R by $j \cdot \Delta R$. Assume that the total number of unit elements (N) is large and that $N \cdot \Delta R \ll R$ to simplify the results.
   a) Derive an expression for the worst case DNL and INL of the DAC. At which taps do they occur?
   b) What is the maximum tolerable relative gradient $\Delta R/R$ in percent that yields a worst case INL of less than 0.5 LSB for a 12-bit DAC?