

Homework 5

Due Tuesday April 15, 2008

1. You are to design three aspects of a fully differential folded-cascode amplifier with PMOS inputs. You may use ideal current sources (shunt with large resistor in case of convergence problems) for M3-M6 and M11 (omit cascodes M9, M10, M12) and an ideal CMFB (built with Voltage Controlled Current Sources, VCCS) except when stated otherwise. Use the high swing cascode bias circuit or ideal voltage sources for biasing. Embed the amplifier into a fully differential feedback network with $C_L=5\text{pF}$, $C_s=400\text{fF}$, $C_f=100\text{fF}$.

Annotate all SPICE plots with:

- Specification (red): indicate “forbidden”, i.e. out-of-spec region, which the simulation result should not traverse
- Hand-analysis (green)
- Computer simulation (black): set appropriate scale so that spec is easily verifiable. Mark axes.
- Other annotation and comments (blue)

- a) **Stability:** find the width of M1, M2, M7, M8 and all bias currents such that $g_{m1}=10\text{mS}$ and $g_m/I_D=10\text{V}^{-1}$. $L=0.5\mu\text{m}$. Plot (with SPICE) both DC and small signal low-frequency open-loop differential mode gain A_{dm} versus V_{od} . Then close the feedback loop and calculate the loop-gain $T_{dm}(s)$ and the phase margin. Verify with SPICE.
- b) **CMFB:** replace the current source simulating M11 with a transistor and add a capacitive CMFB from the amplifier output to the gate of M11. Dimension all devices such that the loop bandwidth of the CMFB is at least 50% of the amplifier differential-mode loop-gain bandwidth. Perform the following checks with SPICE:
- .dc analysis of V_{oc} versus V_{GS11} .
 - .ac analysis of loop-gain. What is the phase margin?
 - .tran V_{od} and V_{oc} versus time for an input step with $V_{id}=1\text{V}$.
- c) **Settling:** Find the minimum biasing current and g_{m1} required (g_m/I_D not necessarily 10V^{-1}) for a dynamic settling error $\varepsilon=0.05\%$, $t_s=50\text{ns}$, and $V_{id,step}=500\text{mV}$. Verify with SPICE (plot zoomed version of dynamic error and current at output of amplifier).
- d) **Noise:** Revert to circuit from part (a) but realize the current sources (and their cascodes) with real transistors with $g_m/I_D=5\text{V}^{-1}$ ($L=0.5\mu\text{m}$). Find g_{m1} (change W and I_D compared to part (a)), C_L , C_s and C_f such that the peak SNR at the amplifier output (with feedback) is 90dB. Use $V_{od,max_peak_peak}=2.8\text{V}$ ($V_{DD}=3\text{V}$).

