Homework 1
Due Tuesday February 5, 2008

For the following questions, use the EECS 240 180nm CMOS process technology. Unless otherwise specified, use a transistor with W = 10μ, L= 0.18 μ. For some questions, you need to access internal device parameters such as gm or V_{Th} . Each simulator has a specific way of doing this.

To access the DC parameters in a sweep in Spectre, you need a statement "save MX:all" in your netlist, where MX is the transistor in question. The results of the sweep can be accessed through the results browser (not the waveform calculator), and the save statement can be case sensitive.

In HSPICE, you need to use the .probe card to save specific things. An example would be: `.probe vstar=par('2*i(m1)/gmo(m1)')` Parameters other than gm can be saved in the same way, and a list of parameter names can be found in the HSPICE manual.

Other simulators may be able to do this. If your simulator cannot perform this task, it will be unable to be used in this course.

1. Plot the threshold voltage of an NFET and PFET as a function of channel length L. What causes the variation in V_{Th} ?

2. (NFET) Plot the gm versus V_{GS} of the transistor on a linear and log scale. Compare the results with a simple square law and sub-threshold model. Bias the transistor with $V_{GS} = V_{DS}$.

3. Plot the total gate capacitance of a NFET configured as a MOS capacitor. Vary the V_G to cover accumulation, depletion, and inversion. Is the capacitance in the inversion region constant? Why?

4. (NFET) Plot the output resistance r_o and DC gain $g_m r_o$ versus V_{DS}. To maintain a DC gain of 80% of the peak value, what is the allowed output swing? Bias the transistor with V* = 200mV. What is λ?

5. (NFET and PFET) Plot g_m/I_D, f_T and the product of the two as a function of V^* for L=180nm, 250nm, and 500nm. What are the maximum g_m/I_D, f_T, and "optimal" V^* for each channel length? Set $V_{DS}=V_{GS}$ and vary V^* from 0 to 500mV. For V^*=200mV, plot the f_T versus L.

6. (NFET and PFET) Plot I_D versus V^* for L=180nm, 250nm, and 500nm. Set $V_{DS}=V_{GS}$ and vary V^* from 0 to 500mV.

7. What is the minimum drain current needed to bias a 10/0.18 NMOS device in strong inversion? For the device to be clearly in strong inversion, V* must be at least 150mV.