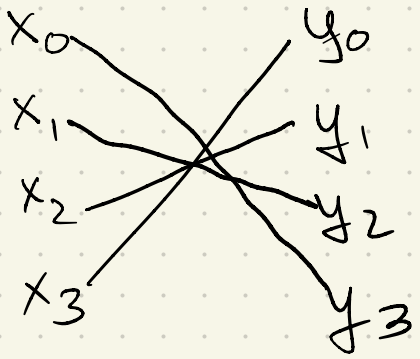
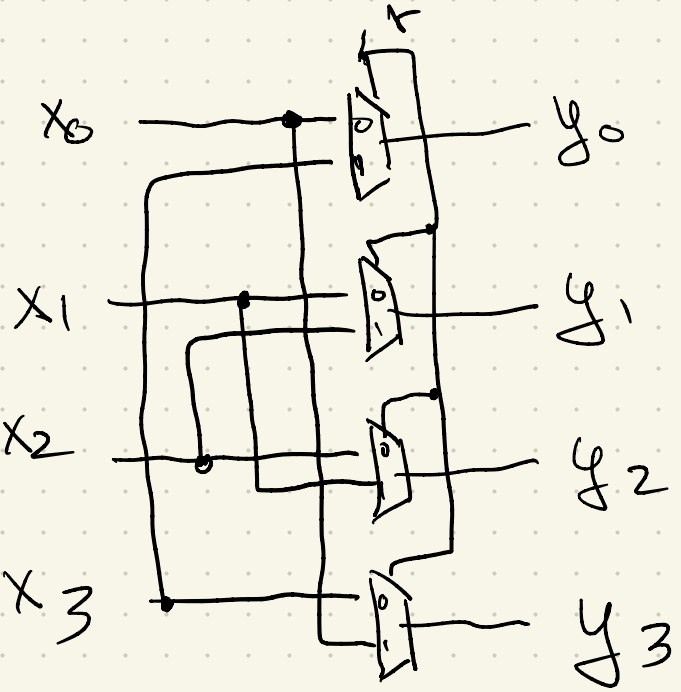
#3 Bit Reverser

Bit reversal can be acheived by wiring only:



Conditional bit reversal uses muxes:



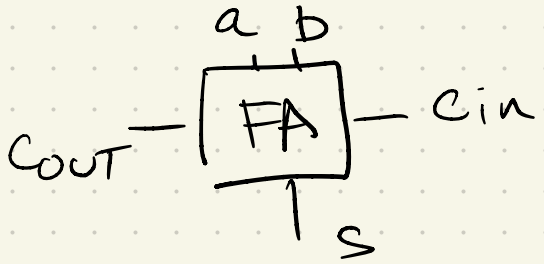
Logic delay involves just the single mux $\therefore \tau = \Theta(1)$

Wire delay involves at least 1 wire whose length is $\propto n$. Wire delay is $\propto \text{length}^2 \therefore \hat{\tau} = \Theta(n^2)$

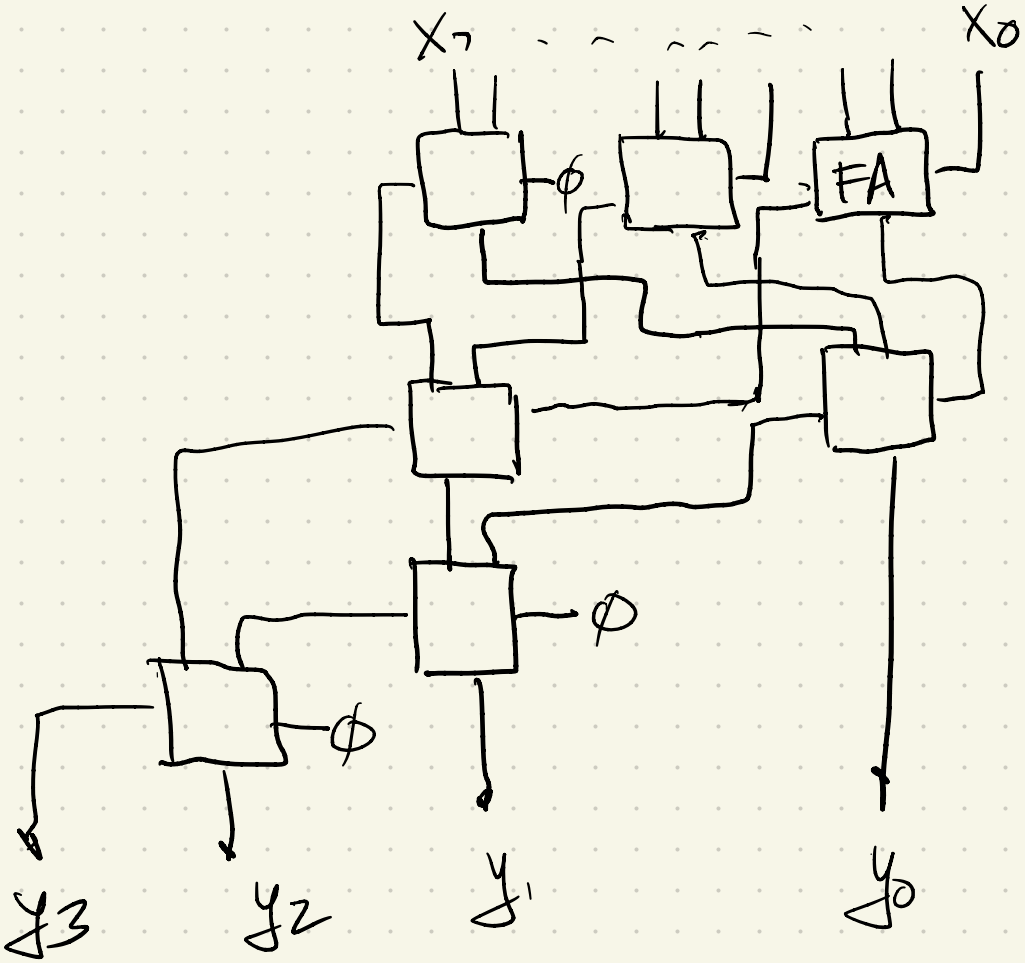
#2 Pop Count

Just need to sum up all the bits - but must preserve the correct bit "significance".

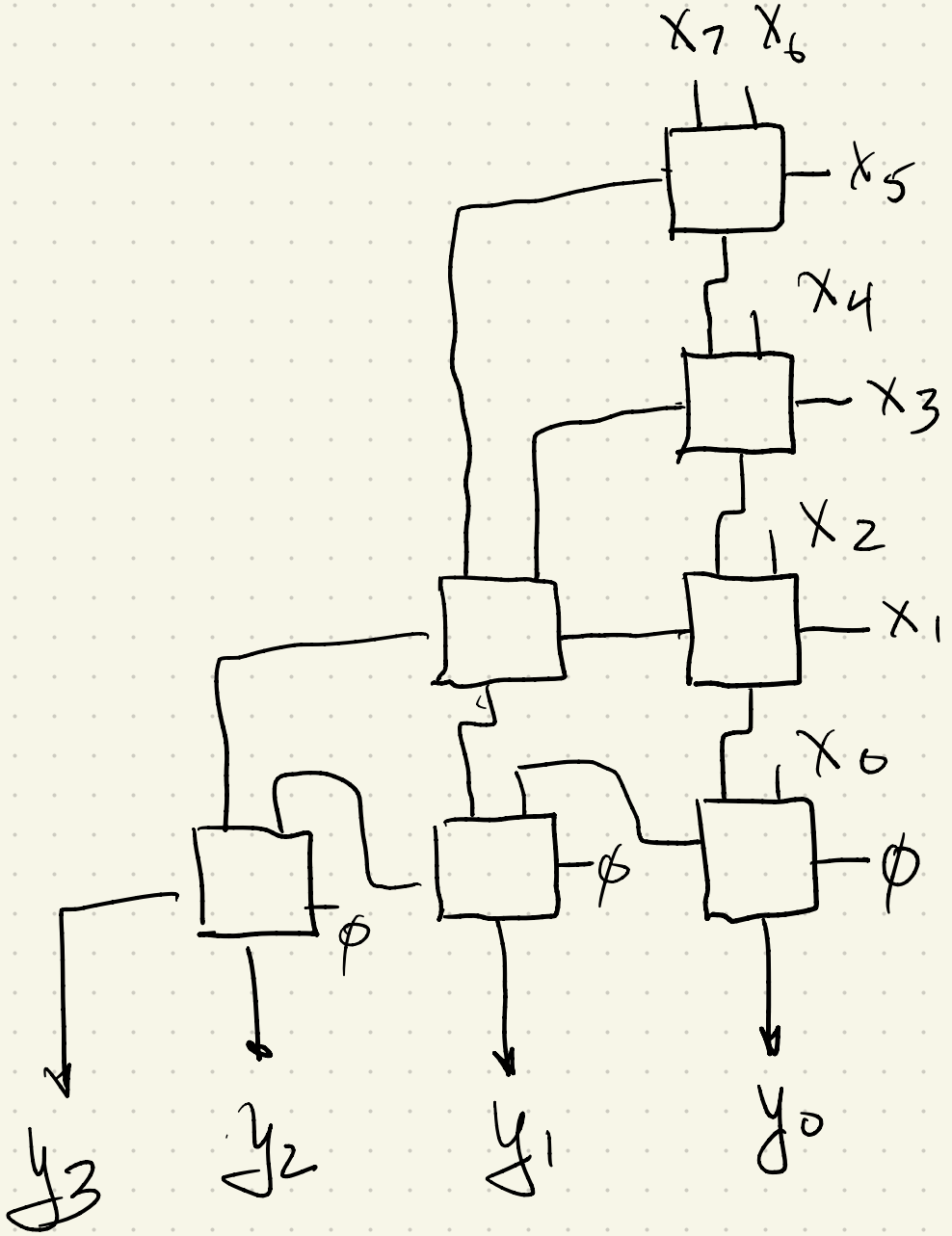
Here are 2 possible solutions using just FA cells.



Output must be 4 bits.

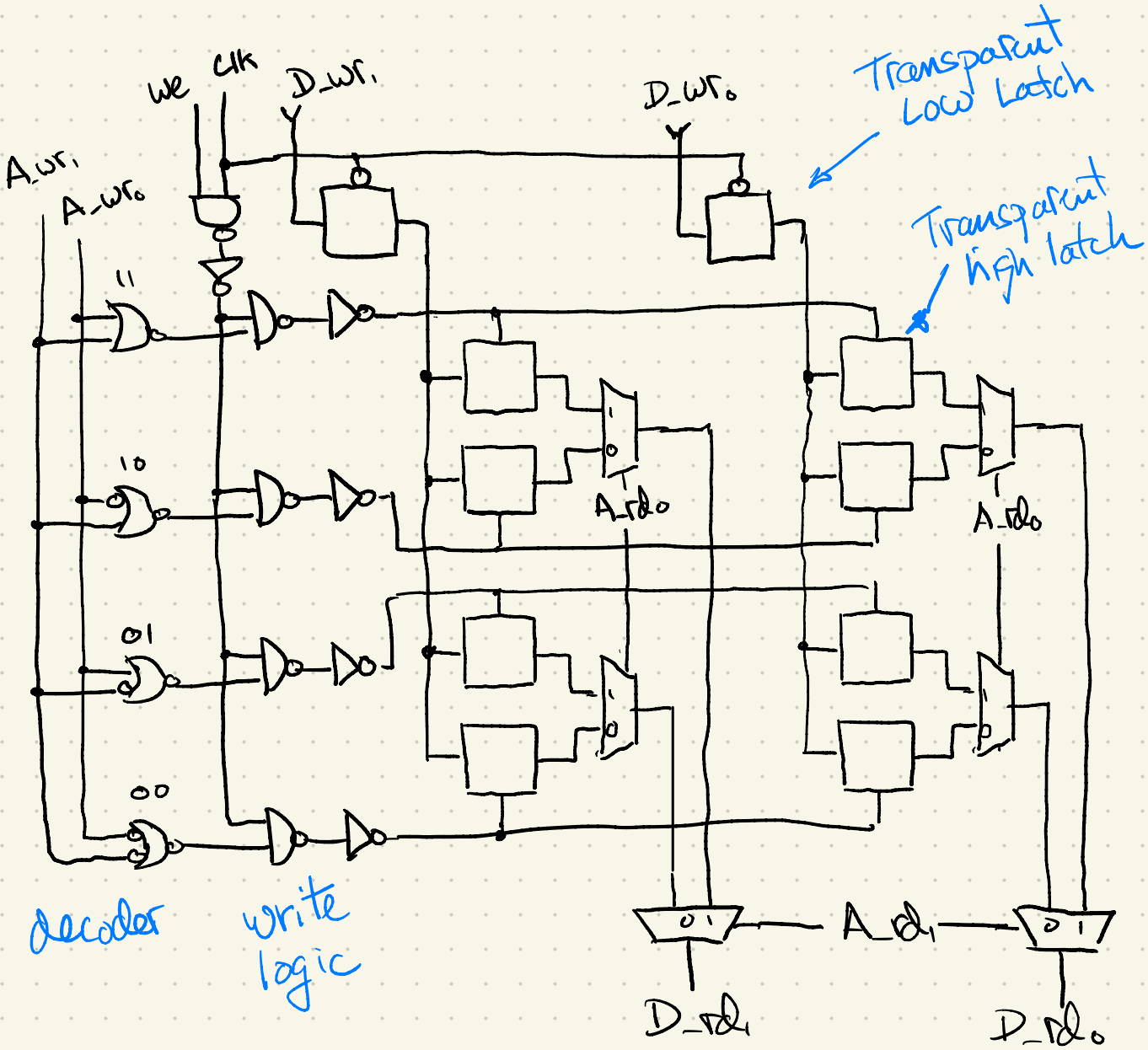


#3



Remember Cout has 2X significance of S.

#1 Register File



#1

Notes:

- Multiple options exist for implementation of decoder, write enable & row select logic for write.
- Reading must be mux based - tri-states permitted.
- Best solution uses "split FF design".
  2 Transparent low input latches then 8 transparent high latches in the array OR
  8 transparent low latches in the array & 2 transparent high latches at output.