EECS 151/251A Homework 9

Due Monday, April 24, 2023

Problem 1: List Processor

We would like to evaluate the list processor architectures in the lecture slides using the FOM (figure of merits). The FOM here is performance (nodes per second) divided by cost, where the cost of each component is given in the table below. For this problem, ignore the delay and cost of control logic. Use 16-bit components for the sum part (15-bit is enough though).

component	delay (ns)	cost
N-bit register with CE	$t_{clk-q} = t_{setup} = 0.5$	$16N + 6$
N-bit multiplexer	1	$8N + 2$
N-bit adder	$2\log_2(N) + 2$	$36N - 12$
Memory	10 for async read	0
N-bit zero comparator	$0.5\log_2(N)$	$4N - 4$

(a) Draw a circuit diagram for an 8-bit zero comparator based on the delay and cost in the table. Note that the cost is the number of transistors.

(b) Formulate the FOM in terms of NPC (nodes per cycle), T (clock period), and the number of components shown below.

component	number
8-bit register with CE	a
16-bit register with CE	b
8-bit multiplexer	c
16-bit multiplexer	d
8-bit adder	e
16-bit adder	f
8-bit zero comparator	g

(c) Fill out the following table for the list processor architectures in the lecture slides.

Architecture	NPC	T (ns)	a	b	c	d	e	f	g	FOM
1										
2										
3										
4										

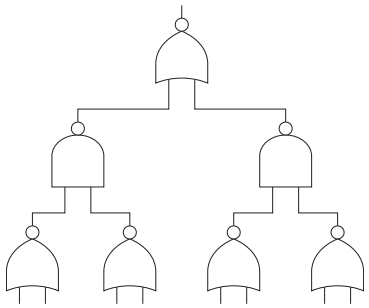
(d) Would it help if nodes are aligned in memory for the first architecture? The address of the next node is always stored at an even address. Explain why or why not.

(e) Design a list processor with 32×16 memory and maximize the FOM. The memory stores the value and the next address of a node at the same address and has 10 ns acync-read delay. Use 8-bit components for the address part. No need to design a control logic. What is the maximized FOM of your design?

(f) Would it help if the 32×16 memory has multiple ports? Explain why or why not.

Solution:

(a)



(b)

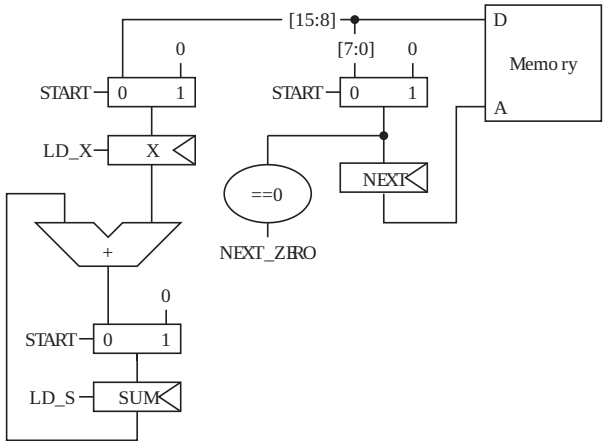
$$\text{FOM} = \frac{\text{NPC}}{\text{T}} \times \frac{1}{134a + 262b + 66c + 130d + 276e + 564f + 28g}$$

(c)

Architecture	NPC	T (ns)	a	b	c	d	e	f	g	FOM
1	0.5	31	1	1	2	1	1	1	1	10,569
2	0.5	23	2	1	3	1	1	1	1	12,595
3	0.5	23	2	1	3	2	0	1	1	13,759
4	0.5	13	3	1	5	2	0	1	1	20,835

(d) It helps because then we can replace the adder for address by an OR gate, which reduces the critical path delay as well as the cost.

(e)



NPC	T (ns)	a	b	c	d	e	f	g	FOM
1	12	2	1	2	1	0	1	1	60,212

(f) It doesn't help because we don't have an address of the next node.

Problem 2: Inverter Power

Consider an inverter with 10 fF load capacitance including the parasitic capacitance. Assume V_{dd} is 0.9 V.

(a) When the output of the inverter changes from 0 to 1, how much energy is dissipated?

(b) When the output of the inverter changes from 1 to 0, how much energy is dissipated?

(c) If the input of the inverter is the clock signal, how much power does it consume? Assume clock period is 1 ns.

(d) If the input of the inverter flips on a positive clock edge with the probability $\alpha = 0.1$, how much power is it expected to consume? Assume clock period is 1 ns.

Solution:

(a)
Energy charged in the capacitor:

$$\int IVdt = \int \frac{dQ}{dt}Vdt = \int C\frac{dV}{dt}Vdt = \int_0^{V_{dd}} CVdV = \frac{1}{2}CV_{dd}^2$$

Energy provided from source:

$$\int IV_{dd}dt = V_{dd}\int C\frac{dV}{dt}dt = V_{dd}\int_0^{V_{dd}} CdV = CV_{dd}^2$$

Energy dissipated:

$$CV_{dd}^2 - \frac{1}{2}CV_{dd}^2 = \frac{1}{2}CV_{dd}^2 = 4.05 \text{ fJ}$$

(b)

$$\frac{1}{2}CV_{dd}^2 = 4.05 \text{ fJ}$$

(c)

$$\frac{1}{2}CV_{dd}^2 \times 2f = CV_{dd}^2 f = 8.1 \text{ µW}$$

(d)

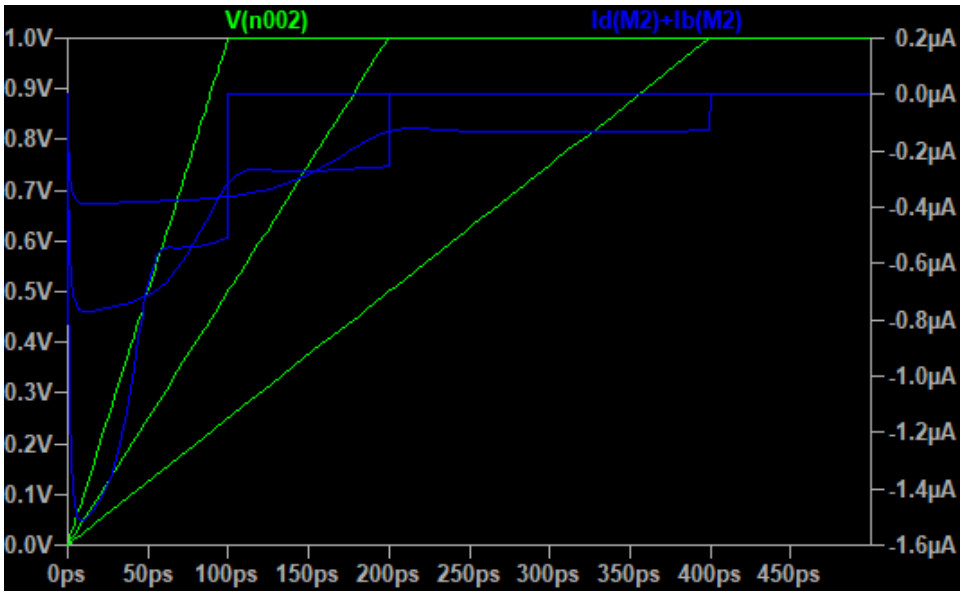
$$\frac{1}{2}\alpha CV_{dd}^2 f = 405 \text{ nW}$$

Problem 3: Short Circuit Power

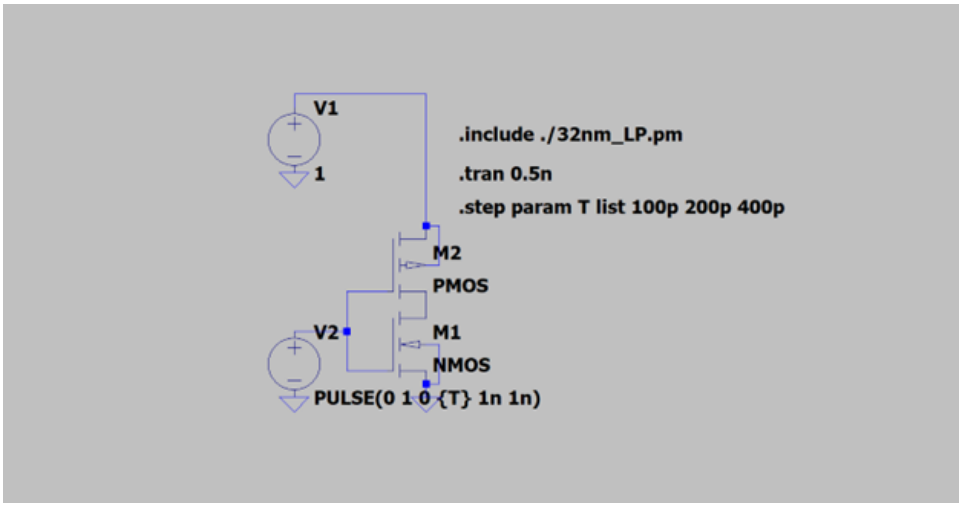
Set up a simulation in LTSpice to demonstrate short-circuit power. Build an inverter with $WP = 2WN = 0.1$ µm and $LN = LP = 32$ nm at a $V_{dd} = 1$ V. Set up the schematic to have input transitions of 100 ps, 200 ps, and 400 ps. To measure the short circuit current, see how much current is conducting through the PMOS for a high-to-low transition. Please turn in a screenshot of your schematic as well as a waveform of the three short-circuit currents.

Solution:

Waveform:



Schematic:



Problem 4: Switching Activity Analysis

(a) A signal a takes 0 or 1 with the same probability (0.5) for each cycle, regardless its previous value. What is the probability that a flips between two consecutive cycles?

(b) Consider a 2-input AND gate with input a_0 and a_1 and output b. a_0 and a_1 are independent and satisfy the same condition as a above. What is the probability that b flips between two consecutive cycles?

(c) Consider a 2-input OR gate with b_0 and b_1 and output c. b_0 and b_1 are independent and satisfy the same condition as b above. What is the probability that c flips between two consecutive cycles?

Solution:

(a)

$$\frac{1}{2}\cdot\frac{1}{2}+\frac{1}{2}\cdot\frac{1}{2}=\frac{1}{2}$$

(b) b is 1 with the probability 1/4 regardless its previous value.

$$\frac{1}{4}\cdot\frac{3}{4}+\frac{3}{4}\cdot\frac{1}{4}=\frac{3}{8}$$

(c) c is 1 with the probability 7/16 regardless its previous value.

$$\frac{7}{16}\cdot\frac{9}{16}+\frac{9}{16}\cdot\frac{7}{16}=\frac{63}{128}$$