

EECS 151/251A Homework 7

Due Monday, April 3, 2023

Problem 1: Tradeoffs

The execution time of program is expressed as

$$\#instructions \times CPI \times Clock\ period. \quad (1)$$

Imagine we have designed a microarchitecture of 3-stage RISC-V CPU, which resolves all hazards by stalling. For each of the following changes, explain its effect over $\#instructions$, CPI, clock period, and overall performance.

1. Use CISC (e.g. memory-to-memory instructions) instead of RISC. Assume we maintain the clock period.
2. Implement forwarding.
3. Implement a branch predictor.
4. Implement 5-stage pipelining.
5. Implement superscaler (execute multiple instructions at a time).
6. Implement cache (assume the original microarchitecture does memory access in one cycle).

Problem 2: Orthogonal Instruction Encoding

The table below shows the types of base instructions in RICS-V ISA. Assume immediates will be sorted and sign-extended properly in microarchitecture. In this encoding, some bits are used for multiple purposes e.g. bit 7 is used for two purposes: `rd` and `imm`. If we use each bit only for one purpose, how many bits do we need for one instruction? Your encoding must cover all RV32I base instructions except `FENCE`, `ECALL`, and `EBREAK`. Merge opcode and functs and give a new encoding to minimize the bit-width.

Hint 1: we need 20 bits for `imm`.

Hint 2: `shamt` is included in `imm`.

31	27	26	25	24	20	19	15	14	12	11	7	6	0	
funct7				rs2		rs1		funct3		rd		opcode		R-type
imm[11:0]						rs1		funct3		rd		opcode		I-type
imm[11:5]				rs2		rs1		funct3		imm[4:0]		opcode		S-type
imm[12:10:5]				rs2		rs1		funct3		imm[4:1 11]		opcode		B-type
imm[31:12]										rd		opcode		U-type
imm[20 10:1 11 19:12]										rd		opcode		J-type

Problem 3: Memory Address

Imagine you are asked to design a 1 MByte memory with $2N$ rows and N bits per row. Determine N and calculate how many bits you need for the row select signal and the column select signal. The row select signal selects one row, and the column select signal extracts one Byte from the selected row.

Problem 4: Predecoder

Calculate the area of 16-bit decoder for 1-level, 2-level, and 4-level implementations. The 1-level implementation uses one 16-input AND gate for each output. The 2-level implementation has two levels of 4-input AND gates. The 4-level implementation has four levels of 2-input AND gates. Assume the area taken by a N -input AND gate is N , and inverters do not contribute to the area.