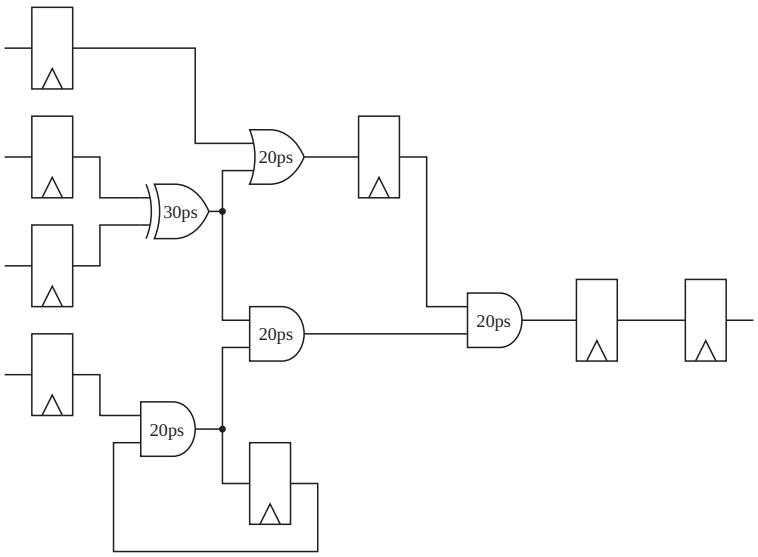
EECS 151/251A Homework 6

Due Monday, Mar 6, 2023

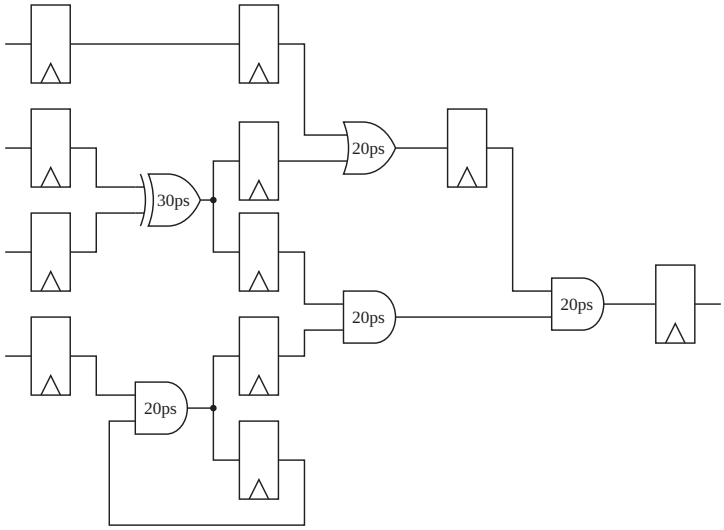
Problem 1: Retiming

Consider the circuit below. What is the maximum clock frequency? Retime the circuit to minimize the critical path delay. What is the maximum clock frequency for the retimed circuit? Also show the diagram of the retimed circuit. The FFs have $t_{setup} = 10$ps, $t_{clk-q} = 10$ps, and $t_{hold} = 5$ps.

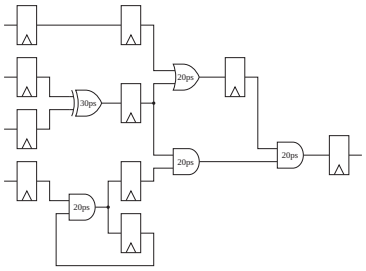


Solution:

Original maximum clock frequency: $\frac{1}{10+10+30+20+20\text{ps}} \approx 11.1$GHz.
(The hold time constraint does not matter because clock to q delay is larger.)
Retimed maximum clock frequency: $\frac{1}{10+10+20+20\text{ps}} \approx 16.6$GHz.
Diagram:



Note: The following diagram is wrong because it merges two FFs at the fanout of XOR gate even though we are not given initial values of FFs.



Problem 2: Inverter Chain

Design an inveter chain that drives an output load of 4096fF with the minimum delay. The input capacitance of the first inverter must be 1fF. The technology has $\gamma = 1.5$. Report the number of inverters and their relative sizes. You may use the following approximation:

$$f = e^{(1+\frac{1.5}{f})} \Leftrightarrow f \approx 4$$

(You don't have to preserve the function i.e. you may use odd number of inverters.)

Solution:

Using $F = \frac{4096}{1} = 4096$, the minimum total delay using N inverters is

$$t_{total} = N \cdot t_{inv}(1 + \frac{\sqrt[N]{F}}{\gamma}).$$

As given in the lecture, $f = \sqrt[N]{F}$ that minimizes the total delay is given by

$$f = e^{(1+\frac{\gamma}{f})}.$$

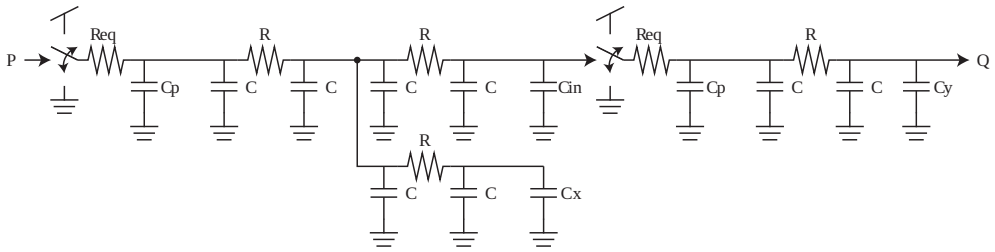
With $\gamma = 1.5$, $f \approx 4$. Solving the equation for N,

$$4 = \sqrt[N]{4096} \Leftrightarrow N = 6.$$

So, the answer is a chain of 6 inverters with relative sizes {1, 4, 16, 64, 256, 1024}.

Problem 3: Elmore Delay

Calculate the Elmore delay that a signal takes to propagate from P to Q in the following circuit. Let $\ln 2 = 0.69$.



Solution:

Delay from P to the internal gate:

$$\begin{aligned} t_{PR} &= 0.69R_{eq}(C_p + C + C + C + C + C_{in} + C + C + C_x) \\ &\quad +0.69R(C + C + C + C_{in} + C + C + C_x) \\ &\quad +0.69R(C + C_{in}) \\ &= 0.69R_{eq}(6C + C_p + C_{in} + C_x) + 0.69R(6C + 2C_{in} + C_x) \end{aligned}$$

Delay from the internal gate to Q:

$$\begin{aligned} t_{RQ} &= 0.69R_{eq}(C_p + C + C + C_y) \\ &\quad +0.69R(C + C_y) \\ &= 0.69R_{eq}(2C + C_p + C_y) + 0.69R(C + C_y) \end{aligned}$$

Delay from P to Q:

$$\begin{aligned} t_{PQ} &= t_{PR} + t_{RQ} \\ &= 0.69R_{eq}(8C + 2C_p + C_{in} + C_x + C_y) + 0.69R(7C + 2C_{in} + C_x + C_y) \end{aligned}$$

Problem 4: Wire Rebuffering

We have a 1mm wire driven by a minimum-sized inverter and driving 1fF capacitance at the other end. The minimum-sized inverter has 500 Ω resistance, 1fF input capacitance, and 1fF parasitic capacitance. The wire has 2 kΩ/m resistivity and 50 nF/m capacitivity. You are going to minimize the delay of this wire by inserting minimum-sized inverters. How many minimum-sized inverters

would you insert? (You don't have to preserve the function i.e. you may insert odd number of inverters.)

Solution:

Delay after inserting $N-1$ inverters is

$$N(R_{inv}(C_p + \frac{C_w}{N} + C_{in}) + \frac{R_w}{N}(\frac{C_w}{2N} + C_{in})).$$

Its derivative is

$$R_{inv}(C_p + C_{in}) - \frac{R_w C_w}{2N^2}.$$

This derivative is 0 when

$$N = \sqrt{\frac{R_w C_w}{2R_{inv}(C_p + C_{in})}}.$$

By assigning $R_{inv} = 500\Omega$, $C_p = C_{in} = 1\text{fF}$, $R_w = 2\Omega$, and $C_w = 50,000\text{fF}$,

$$N = \sqrt{\frac{2 \times 50,000}{2,000}} = \sqrt{50} \approx 7.$$

Therefore, we need to insert 6 ($= N-1$) inverters to minimize the delay.

Problem 5: Transistor Sizing

Angela is designing a full custom IC and has the idea that, when she does the chip layout, if she doubles the strength of all the transistors in the design (by drawing the layout with twice the nominal transistor widths), that she can speed up the circuit operation. Her friend John says that the 2X wider transistors will not improve the speed. What is your opinion?

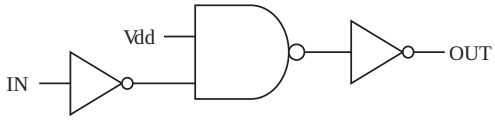
Solution:

Naive answer:
Doubled transistor width decreases its resistance by half but doubles its capacitance. Since the delay is given by product of resistance and capacitance, the minimum inverter delay will remain the same. On the other hand, the wire length won't double if designed carefully, therefore these wider transistors could reduce the total delay.
Advanced answer:
If you layout an extra transistor sharing the drain with the original one, instead of doubling their widths, the parasitic capacitance does not increase. You can reduce gate delay further more by doing this.

Problem 6: Sizing with SPICE

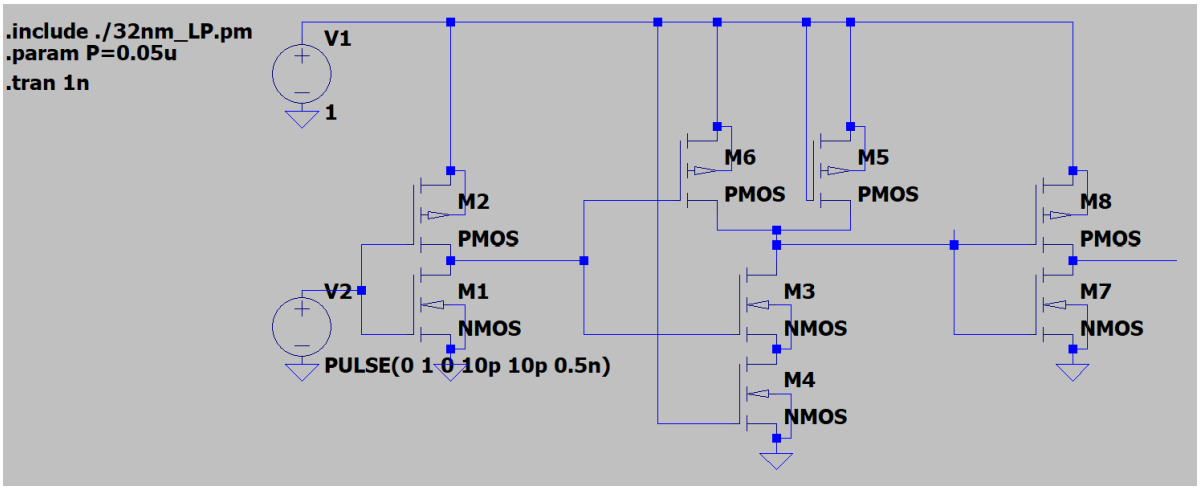
Create the following circuit in SPICE using the 32nm transistor library. The first inverter has 0.05 µm NMOS and 0.1 µm PMOS, while the last inverter has 0.15 µm NMOS and 0.3 µm PMOS. Use 0.15 µm NMOS in the NAND gate. In the NAND gate, assign Vdd to the gate of the NMOS that has GND as a source. Vdd is 1V. Measure low-to-high and high-to-low delay of NAND gate with

0.05 µm, 0.15 µm, and 0.3 µm PMOS. Use the pulse setting `PULSE(0 1 0 10p 10p 0.5n)` given in the discussion slides. Provide a screenshot of your schematic and plots of your simulation.

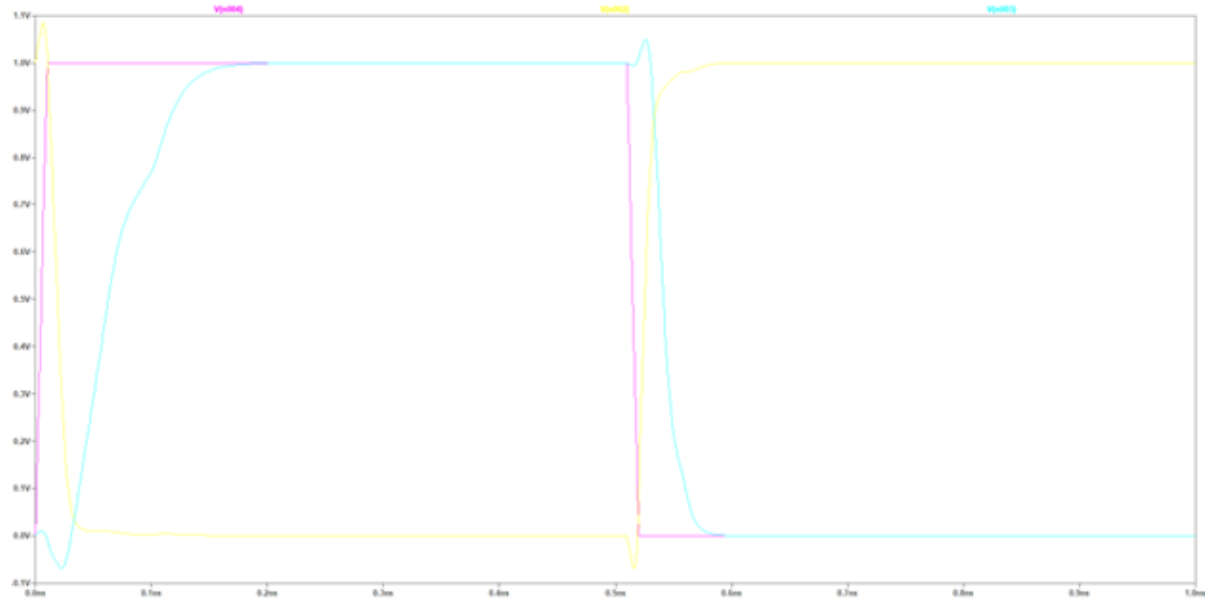


Solution:

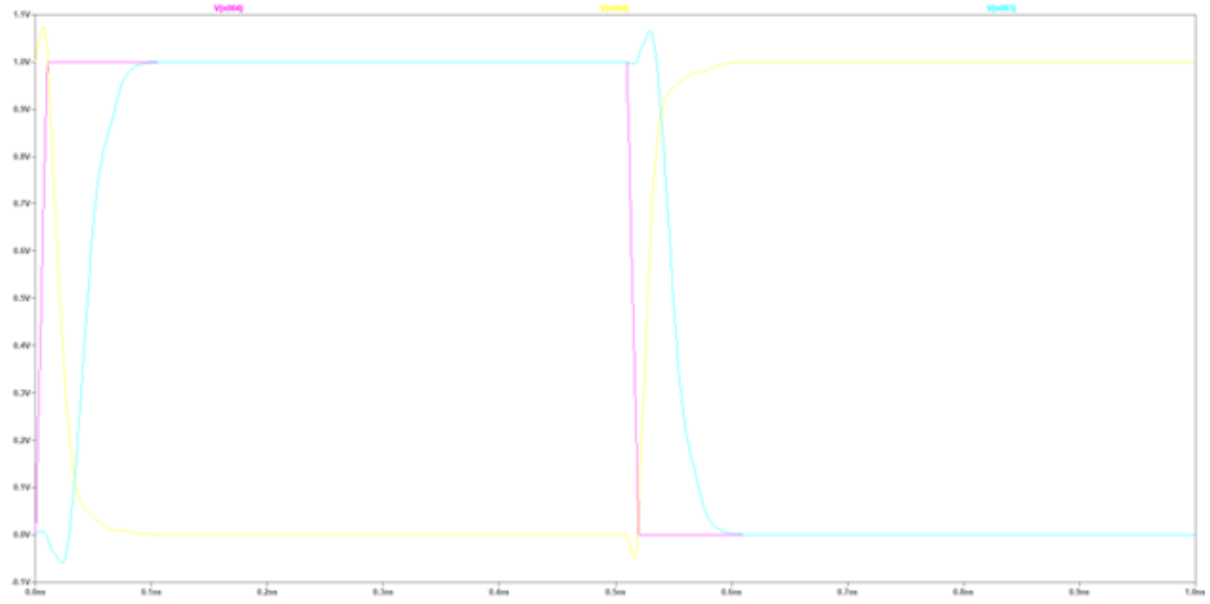
0.05 µm: {Low-to-high delay: 44ps, High-to-low delay: 16ps}
0.15 µm: {Low-to-high delay: 24ps, High-to-low delay: 22ps}
0.30 µm: {Low-to-high delay: 22ps, High-to-low delay: 30ps}
Schematic:



0.05 µm plot:



0.15 µm plot:



0.30 µm plot: