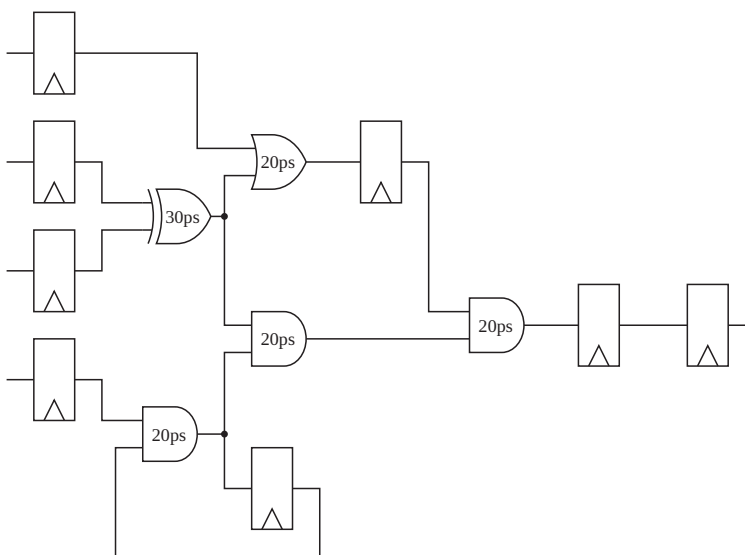# EECS 151/251A Homework 6

Due Monday, Mar 6, 2023

Problem 1: Retiming

Consider the circuit below. What is the maximum clock frequency? Retime the circuit to minimize the critical path delay. What is the maximum clock frequency for the retimed circuit? Also show the diagram of the retimed circuit. The FFs have $t_{setup} = 10$ps, $t_{clk-q} = 10$ps, and $t_{hold} = 5$ps.


Problem 2: Inverter Chain

Design an inveter chain that drives an output load of 4096fF with the minimum delay. The input capacitance of the first inverter must be 1fF. The technology has $\gamma = 1.5$. Report the number of inverters and their relative sizes. You may use the following approximation:

$$f = e^{(1 + \frac{1.5}{f})} \Leftrightarrow f \approx 4$$

(You don't have to preserve the function i.e. you may use odd number of inverters.)

Problem 3: Elmore Delay

Calculate the Elmore delay that a signal takes to propagate from P to Q in the following circuit. Let $\ln 2 = 0.69$.
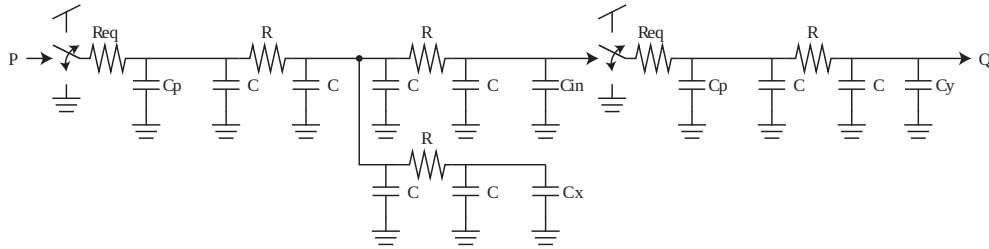
Problem 4: Wire Rebuffering

We have a 1mm wire driven by a minimum-sized inverter and driving 1fF capacitance at the other end. The minimum-sized inverter has 500 Ω resistance, 1fF input capacitance, and 1fF parasitic capacitance. The wire has 2 kΩ/m resistivity and 50 nF/m capacitivity. You are going to minimize the delay of this wire by inserting minimum-sized inverters. How many minimum-sized inverters would you insert? (You don't have to preserve the function i.e. you may insert odd number of inverters.)

Problem 5: Transistor Sizing

Angela is designing a full custom IC and has the idea that, when she does the chip layout, if she doubles the strength of all the transistors in the design (by drawing the layout with twice the nominal transistor widths), that she can speed up the circuit operation. Her friend John says that the 2X wider transistors will not improve the speed. What is your opinion?

Problem 6: Sizing with SPICE

Create the following circuit in SPICE using the 32nm transistor library. The first inverter has 0.05 µm NMOS and 0.1 µm PMOS, while the last inverter has 0.15 µm NMOS and 0.3 µm PMOS. Use 0.15 µm NMOS in the NAND gate. In the NAND gate, assign Vdd to the gate of the NMOS that has GND as a source. Vdd is 1V. Measure low-to-high and high-to-low delay of NAND gate with 0.05 µm, 0.15 µm, and 0.3 µm PMOS. Use the pulse setting PULSE(0 1 0 10p 10p 0.5n) given in the discussion slides. Provide a screenshot of your schematic and plots of your simulation.