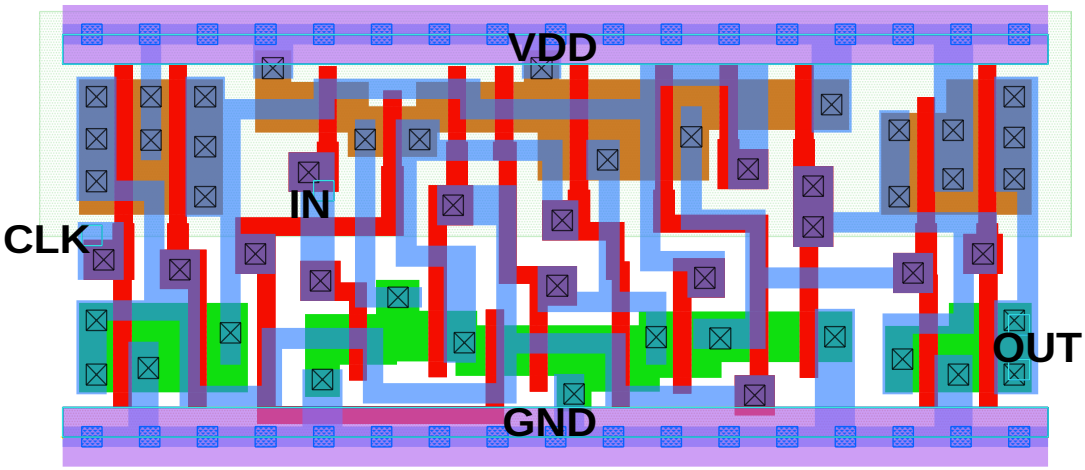
EECS 151/251A Homework 5

Due Monday, Feb 27, 2023

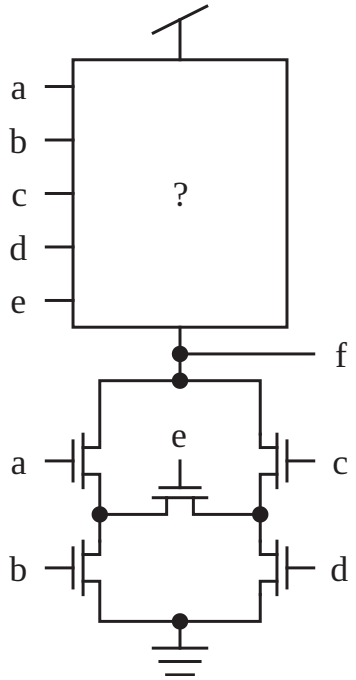
Problem 1: Standard Cell Layout Reverse Engineering

Write a transistor-level schematic of the following layout. What does it implement?



Problem 2: CMOS

Complete the following CMOS schematic with inputs a, b, c, d, e and output f. Also, write a Boolean expression of the output f.



Problem 3: CMOS 2

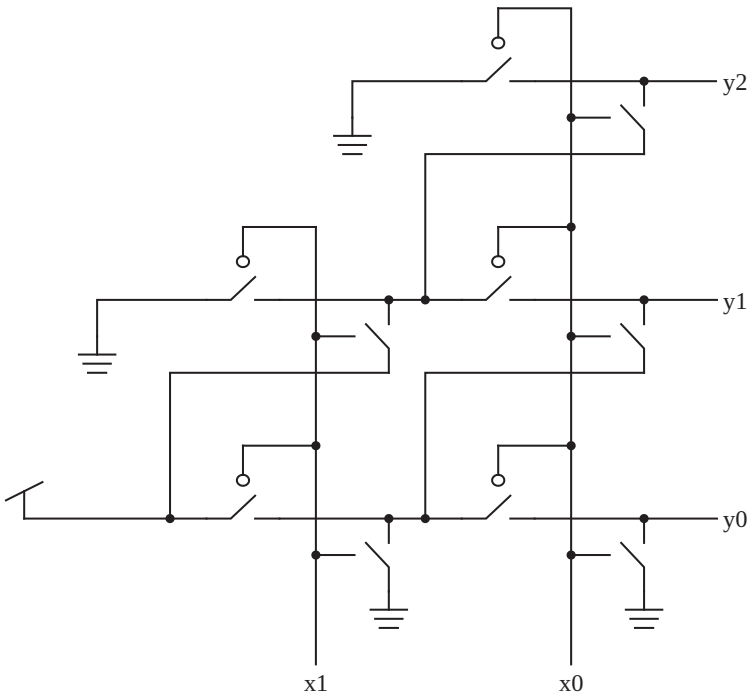
Write a CMOS schematic for $f = a'b' + b'c' + c'a'$.

Problem 4: MOS Characteristics

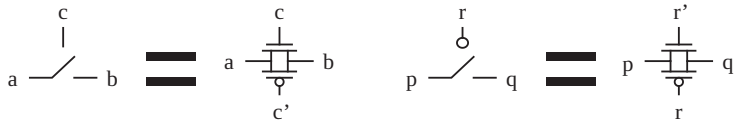
Using **32**nm predictive LTSpice model at `http://ptm.asu.edu/modelcard/LP/32nm_LP.pm` (**this is different from the one we used in HW1!**), measure I_{DS} vs. V_{DS} for $V_{GS} = \{0\text{V}, 0.1\text{V}, \ldots, 1\text{V}\}$. Sweep V_{DS} from 0V to 1V. Create four plots for {0.1 µm wide NMOS, 0.05 µm wide NMOS, 0.1 µm wide PMOS, 0.05 µm wide PMOS}. Set the volatages to negative for PMOS. Also, attach the screenshot of your schematic.

Problem 5: Switch Network

Write a truth table of the following switch network with inputs x_0, x_1 and outputs y_0, y_1, y_2.



Here, switches are transmission gates as shown below.

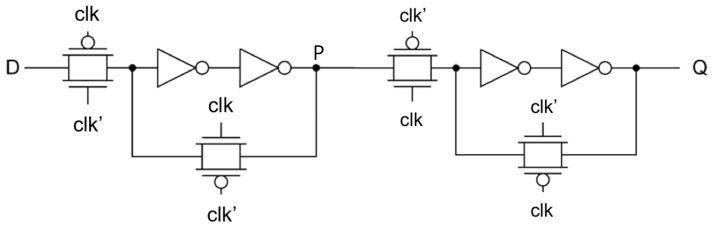


Problem 6: Circular Shifter

Write a schematic of 4-bit circular shifter using only 16 switches and wires (the specification of switches was given in the previous problem). The 4-bit circular shifter performs left circular shifts on a 4-bit input signal `{x3, x2, x1, x0}` and outputs the result as `{y3, y2, y1, y0}`, where the shift amount is given as another 2-bit input signal `{s1, s0}` in a binary number. For example, for input `{x3, x2, x1, x0} = 4'b1001` and `{s1, s0} = 2'd3`, it outputs `{y3, y2, y1, y0} = 4'b1100`.

Problem 7: Delay Flip-Flop

Consider the following flip-flop.



Complete the following waveform for P and Q. Assume each inverter causes 0.5 time unit delay, while transumission gates cause no delay. Dashed lines are written per unit time.