EECS 151/251A Homework 4

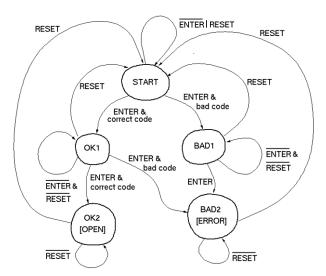
Due Tuesday, Feb 21, 2023

In this homework, you will be asked to use binary-encoded or one-hot-encoded states. In binary encoding, state n corresponds to a state where the FFs hold n in a binary number. For example, in a 4-state machine, the FFs hold 00 in state 0, 01 in state 1, 10 in state 2, and 11 in state 3. On the other hand, in one-hot encoding, state n is a state where the n-th FF holds 1 and the other FFs hold 0. Using the same example, the value of FFs is 0001 in state 0, 0010 in state 1, 0100 in state 2, and 1000 in state 3 in one-hot encoding.

Problem 1: Combinational Lock

IMPORTANT: Use a skeleton at https://inst.eecs.berkeley.edu/~eecs151/sp23/files/ verilog/comb_lock.v for this problem.

Consider the following state transition diagram of a combinational lock.



The following is the additional specification of this combinational lock.

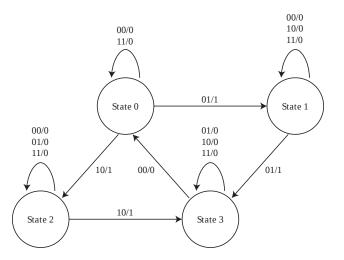
- It receives one 2-bit code at a time.
- The correct code sequence is $11 \rightarrow 10$.
- It outputs two signals: OPEN and ERROR. OPEN is 1 iff it is in OK2, whereas ERROR is 1 iff it is in BAD2.
- It is guaranteed that ENTER and RESET do not take 1 at the same time.

- It uses the following state assignment: {START = state 0, OK1 = state 1, OK2 = state 2, BAD1 = state 3, BAD2 = state 4}.
- (a) Write a Verilog module with binary-encoded states. (*Hint*: Use case.)
- (b) Write a Verilog module with one-hot-encoded states, without using **always** blocks. (*Hint*: Use continuous assignment.)

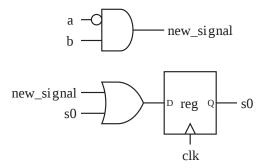
Problem 2: STD to Gate-Level Circuits

Consider the following state transition diagram with input a, b and output o. Labels of the arrow specify the values of input and output as ab/o.

(No need to write Verilog for this problem.)



- (a) Draw a gate-level circuit diagram with binary-encoded states. Use K-maps to simplify the circuit.
- (b) Draw a gate-level circuit diagram with one-hot-encoded states.
- (*Note*: You may omit wires as long as they are named. Example is shown below.)



Problem 3: Alternative Counters

A 2-bit counter is a state machine with 4 states. It transitions from state n to state $(n+1 \mod 4)$ at each positive edge of the clock signal. Assume the states are binary-encoded.

- (a) Write a Boolean expression of the input of each FF.
- (b) Imagine a situation that we need to count 4 cycles but no need to know which cycle we are in of the 4 cycles. In this situation, we can use an alternative counter, which transitions among 4 states in an arbitrary order. For example, it may transition from state 0 to state 2, state 2 to state 1, state 1 to state 3, and state 3 to state 0. Find a best alternative counter in terms of number of 2-input gates, and write the order of states and the Boolean expressions of FF inputs. You cannot use more than two FFs and they are initialized to 0.

Problem 4: Vending Machine

You are to design a control module in a vending machine. The items inside the machine cost \$15, and the machine accepts five dollar and ten dollar bills only. The control module receives two signals that indicate what kind of bill has been deposited.

The control module has three output signals. One signal causes the item to be delivered, while the other two signals cause a bill to be dispensed.

The vending machine has another module that counts the number of five dollar bills inside. The control module receives a signal from it that indicates whether it is out of change or not.

Whenever the amount of money received becomes \$15, the machine delivers the item and resets to its initial state. When it has received \$20, it delivers the item with a change, or returns two ten doller bills if it is out of change. After that, it goes back to the initial state.

Identify your inputs and outputs, and draw a state transition diagram that implements the control module. (No need to write Verilog.)

Assume that only one bill can deposited or dispensed at a time. No bills can be deposited when delivering the item.