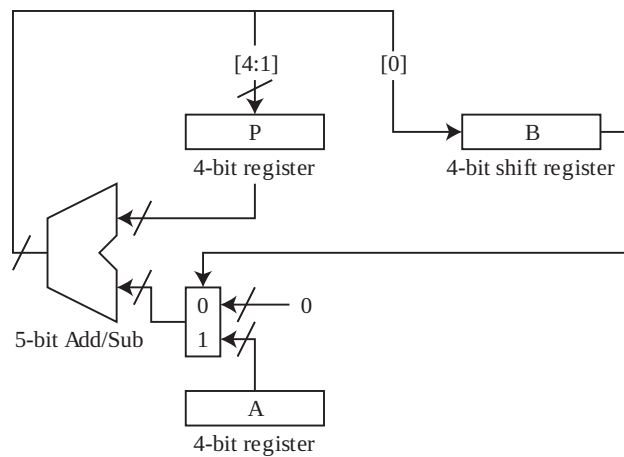


EECS 151/251A Homework 11

Due Monday, May 8, 2023

Problem 1: Signed Shift-and-Add Multiplication

Simulate -3×-5 ($A = -3, B = -5$) on the shift-and-add multiplier shown below. Write down the values of B and P for each cycle. Note that the inputs to the 5-bit Add/Sub are sign-extended, and it performs subtraction only in the last cycle.



Solution:

1. $B = 1011, P = 0000$
2. $B = 1101, P = 1110$
3. $B = 1110, P = 1101$
4. $B = 1111, P = 1110$
5. $B = 1111, P = 0000$

Verify $\{P, B\} = 00001111 = 15$.

Problem 2: Booth's Multiplication Algorithm

Walk through Booth's multiplication algorithm (radix 4) for 8×-9 , where 8 is multiplicand and -9 is multiplier. Show your work.

Solution:

$A = 01000, B = 10111.$

First product: $-01000 = 11000$ since sub A for $\{B_1, B_0, 0\} = 110$

Second product: $(2 * 01000) \ll 2 = 01000000$ since add $2*A$ for $\{B_3, B_2, B_1\} = 011$

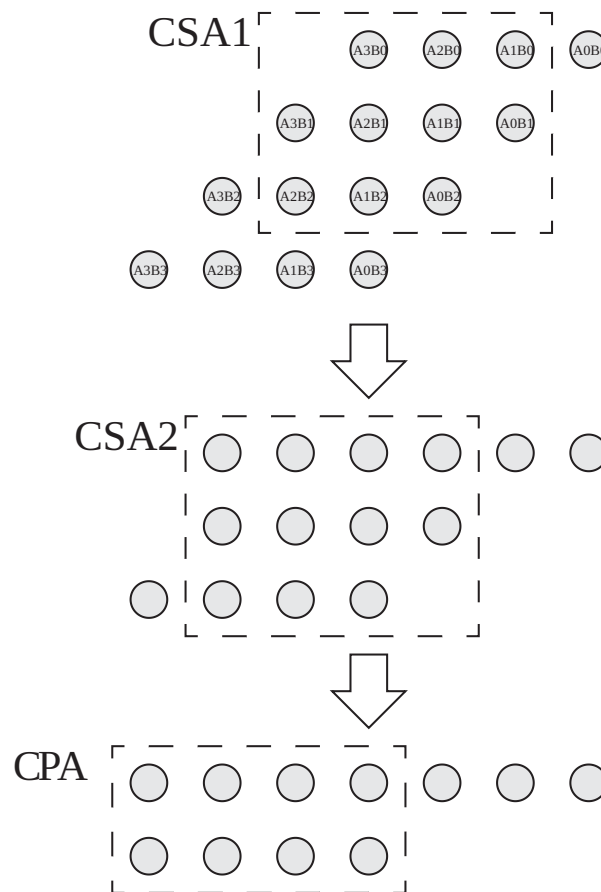
Third product: $(-01000) \ll 4 = 110000000$ since sub A for $\{B_4, B_4, B_3\} = 110$

Result: $1111111000 + 0001000000 + 1110000000 = 1110111000$

Verify $1110111000 = -0001001000 = -72.$

Problem 3: Wallace Tree

The figure below shows the Wallace tree for 4-bit unsigned multiplication. How many FAs and HAs does it use? Do not use FA when there are only 2 bits to add. Use a ripple carry adder for CPA.

**Solution:**

CSA1: 2 FAs, 2 HAs

CSA2: 3 FAs, 1 HA

CPA: 3 FAs, 1 HA

8 FAs and 4 HAs in total.

Problem 4: Constant Coefficient Multiplication

Implement $Z = 945X$ for input X using only 2 subtractors. *Hint: shift by a constant amount is just wiring, does not require any module.*

Solution:

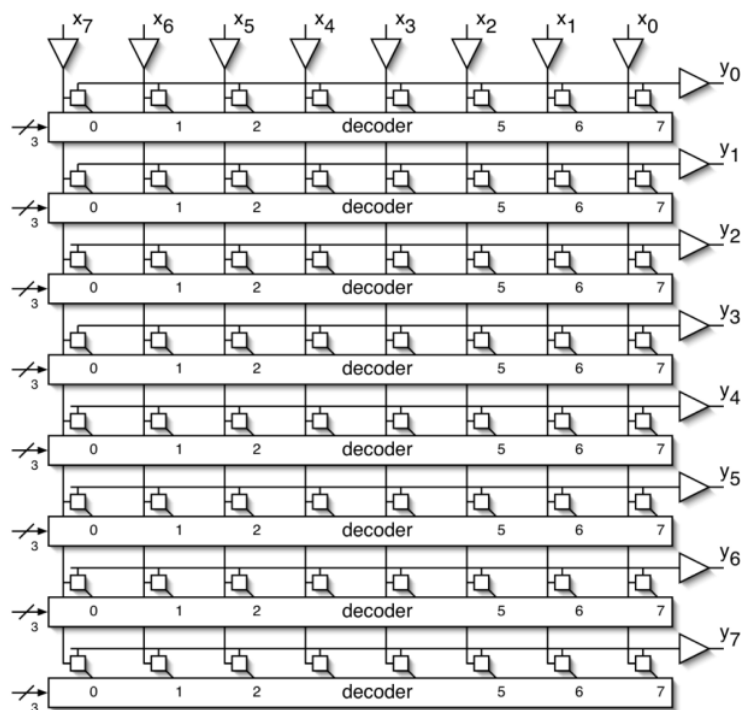
$$945 = 3^3 \times 5 \times 7 = 63 \times 15 = (2^6 - 1) \times (2^4 - 1)$$

$$\text{First module: } Y = (X \ll 4) - X$$

$$\text{Second module: } Z = (Y \ll 6) - Y$$

Problem 5: Cross-bar Switch

How would you configure the decoders in the cross-bar switch below to reverse the order of bits i.e. $y_i = x_{7-i}$ for $i = 0, 1, \dots, 7$?

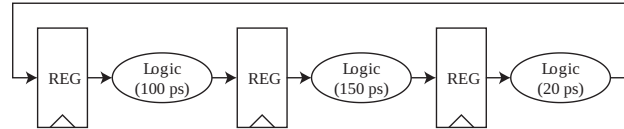


Solution:

From the top, assign $0, 1, \dots, 7$.

Problem 6: Clock Uncertainty

Given setup time 20 ps, clock-to-q delay 10 ps, and cycle-to-cycle jitter 10 ps, what is the maximum frequency of the following circuit by adjusting the clock skew?



Solution:

We can equally distribute the delay between registers by setting the clock skew of the middle register to +10 ps and that of the right register to +70 ps relative to the first register. Then, the delay between registers is $90 + 20 + 10 = 120$ ps. We need additional $2 \times 10 = 20$ ps for jitter, so the maximum frequency is $1/140 = 7.14$ GHz.

Problem 7: Packaging

IC chips need to connect to power supply to be functional. If we are using solder balls (C4) each has 100 pH inductance, how many solder balls do we need to make the voltage fluctuation at most 0.1 V? Assume the maximum current spike is 1.2×10^{11} A/s.

Solution:

$$V_{max} = \frac{L}{N} \cdot \left. \frac{dI}{dt} \right|_{max} = \frac{100 \times 10^{-12}}{N} \cdot 1.2 \times 10^{11} \leq 0.1$$

$$120 \leq N$$