EECS 151/251A Homework 1

Due Monday, Jan 30$^{\text{th}}$, 2023

Problem 1: Pareto Optimal Frontier

John did a design space exploration for his design of a digital widget and came up with the following table of results for frequency (number of operations per sec) in GHz, energy in nanoJoules per operation, and cost as chip area in mm^2. List those rows that represent design points that lie on the Pareto optimal frontier.

(*Update* (1/26): Changed "energy efficiency" to "energy" in the text. It doesn't affect the answer of this problem since the unit is already shown. This change intends to remove the ambiguity of the term "energy efficiency".)

Frequency	Energy	Cost
3	30	4
3	20	3
3	15	3
2	20	3
2	20	2
2	10	1
1	10	2
1	10	1

Problem 2: Dennard Scaling

Imagine the world where Dennard scaling works completely. You were asked to add some features to a processor that originally works at 100MHz with 10W, and the modification you made did not change the frequency but increased the power 20%. If you fabricate this design with a new technology, which has been scaled by a factor of 0.5, what will be the frequency and power consumption?

Problem 3: Die Cost

You are fabricating 150 mm^2 dies on 300 mm wafers with $\alpha = 3$ and a defect per unit area 0.005 /mm^2. Each wafer costs \$20k. How much does each die cost?

Problem 4. Boolean Functions

All functions in this problem are single-output Boolean functions.

(a) How many unique single-input functions exist?

(b) In general, any $(k+1)$-input function can be decomposed into a pair of k-input functions. For example, a function $x(i_0, \ldots, i_k)$ can be decomposed into $y(i_0, \ldots, i_{k-1})$ and $z(i_0, \ldots, i_{k-1})$, where

$$x(i_0, \ldots, i_k) = \begin{cases} y(i_0, \ldots, i_{k-1}) & \text{if } i_k = 0 \\ z(i_0, \ldots, i_{k-1}) & \text{if } i_k = 1 \end{cases}$$

Assume that there are n unique functions with k inputs. How many unique function are there with $k+1$ inputs? Do not use k in your answer. (*Hint*: Consider how many 2-input functions you can compose from unique single-input functions.)

Problem 5. Sequential Logic Circuit

For the sequential logic circuit with input a and output f shown below,
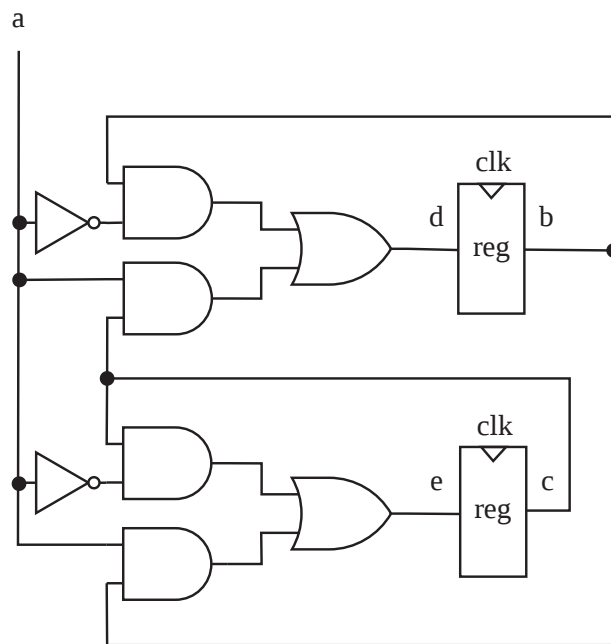
(a) Show the truth table of the combinational part (use a, b, and c as input, and d and e as output).

(b) Complete the following table.

cycle	0	1	2	3	4
a	0	1	1	0	1
b	1	1	0		
c	0	0	1		
d	1	0			
e	0	1			

Problem 6: Rank order for NRE, Recurring Costs, Flexibilty, Performance

Imagine you are designing a product with embedded processing. Your job is to choose the appropriate implementation approach for the processing part of your product. You are given the following choices. Rank order the following design alternatives by filling in the table with 1,2,3,4 representing the relative ranking (1 being the lowest and 4 being the highest). Rank based on the best-case design in each category. If there is a tie, use the lower number (e.g. if tied for 2 or 3, use 2). Flexibility means flexibility after fabrication. Per-die cost of Processor is not required.

	Full-Custom	Std Cell ASIC	FPGA	Processor
NRE Cost				
Performance				
Energy Efficiency				
Per Die Cost				-
Flexibility				

Problem 7: Processor vs. FPGA vs. ASIC

You are the Chief Technical Officer of a new startup, the Orange Scooter Company. As the chief design lead of your (admittedly small) team of engineers, it is up to you to adopt which one from Processors, FPGAs, or ASICs for your upcoming line of scooters. After getting quotes from several foundries and having a chat with the Head of HR about the estimated number of work hours needed for each choice, you arrive at the following conclusions for the NRE and per-unit cost associated with each approach.

	NRE Cost	Per Unit Cost
Processor	$5K	$200
FPGA	$20K	$100
ASIC	$1M	$2

(a) As a small startup, you don't anticipate your first deployment to be too large, and the Head of Marketing (who also happens to be Head of HR) estimates that you will deploy about 100 units in the first quarter. Which type of design would you choose? Why?

(b) In what range of units to deploy would FPGA be the best option?

Problem 8: Voltage Transfer Curve (VTC) of Inverter in SPICE

Using SPICE DC Analysis, plot the VTC of an inverter using the 16nm process technology provided on `http://ptm.asu.edu/modelcard/LP/16nm_LP.pm`. The nominal supply voltage for this process is $0.9\,\mathrm{V}$. Use a length of $16\,\mathrm{nm}$ for both devices and a width of $300\,\mathrm{nm}$ for PMOS and $80\,\mathrm{nm}$ for NMOS. Don't forget to connect the body of the devices to the correct voltages - NMOS body to GND and PMOS body to VDD!

Report the value of output (*vout*) when the input is {0.44V, 0.45V, 0.46V}. What is the approximate slope in the range (0.44V, 0.46V)? For help setting up the simulation, follow the LTspice tutorial on the class website. `https://inst.eecs.berkeley.edu/~eecs151/sp20/files/spice_tutorial.pdf`. You can export the values of datapoints in the plot by **File > Export data as text**.