University of California at Berkeley College of Engineering Department of Electrical Engineering and Computer Science

EECS151/251A - LB, Spring 2023

FPGA Project Report Guidelines

Upon completing the project, you will be required to submit a report detailing the progress of your EECS151/251A project. The report should document your final circuit at a high level, and describe the design process that led you to your implementation. We expect you to document and justify any tradeoffs you have made throughout the semester, as well as any pitfalls and lessons learned (not make excuses for why something didn't work). Additionally, you will document any optimizations made to your system, the system's performance in terms of area (resource use), clock period, and CPI, and the resulting figure-of-merit (FOM) value. Also describe any other information that sets your project apart from other submissions.

The staff emphasizes the importance of the project report because it is the product you are able to take with you after completing the course. All of your hard work should reflect in the project report. Employers may (and have) ask to examine your EECS151/251A project report during interviews. Put effort into this document and be proud of the results. You may consider the report to be your medal for surviving EECS151/251A.

Report Details

You will turn in your project report, as a PDF file, on Gradescope by midnight Monday May 8th. The report should be around 8 pages total with around 5 pages of text and 3 pages of figures (\pm a few pages on each). Ideally you should mix the text and figures together.

Here is a suggested outline and page breakdown for your report. You do not need to strictly follow this outline, it is here just to give you an idea of what we will be looking for.

- Project Functional Description and Design Requirements. Describe the design objectives of your project. You don't need to go into details about the RISC-V ISA, but you need to describe the high-level design parameters (pipeline structure, memory hierarchy, etc.) for this version of the RISC-V. (≈ 0.5 page)
- **High-level organization**. How is your project broken down into pieces. Block diagram level-description. We are most interested in how you broke the CPU datapath and control down into submodules, since the code for the later checkpoints will be pretty consistent across all groups. Please include an updated block diagram (≈ 1 page).
- Detailed Description of Sub-pieces. Describe how your circuits work. Concentrate here on novel or non-standard circuits. Also, focus your attention on the parts of the design that were not supplied to you by the teaching staff. (≈ 2 pages).
- Status and Results. What is working and what is not? At what FOM value is your final design? What is the breakdown of Fmax, cost, and CPI. What was your original FOM value (and breakdown of cost, CPI, and Fmax) before you implemented optimizations? Describe

your optimization approach, including what was effective and what wasn't. For non-working designs, this section is particularly important to help us assign partial credit. If you design is not fully functional, describe what does work, what doesn't, and your best understanding as to what is wrong. ($\approx 1-2$ pages).

- Conclusions. What have you learned from this experience? How would you do it different next time? (≈ 0.5 page).
- Division of Labor. This section is mandatory. Each team member will turn in a separate document from this part only. The submission for this document will also be on Gradescope. How did you organize yourselves as a team. Exactly who did what? Did both partners contribute equally? Please note your team name next to your name at the top. (≈ 0.5 page).

When we grade your report, we will grade for clarity, organization, and grammar. Make sure to proofread and correct mistakes before turning it in. Submit your report to the Gradescope assignment. Only one partner needs to submit the shared report, while each individual will need to submit the division of labor report to a separate Gradescope assignment.