EECS 151 Disc 7

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Contents

- Practice midterm problems

Lookup Tables (SP 20)

FPGAs Logic Block [5pts] Using nothing other than 3-LUTs, demonstrate how you would construct a 6-LUT. Label your inputs $x_0, x_1, ..., x_5$, and output as y.

Lookup Tables (SP 20)

Static CMOS Gates (SP 21)

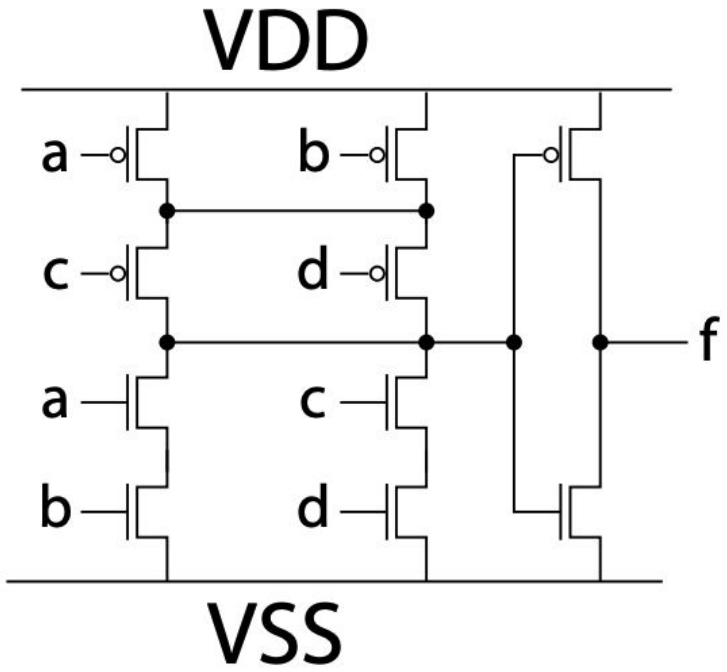
In this problem you are asked to design and analyze a 4-input static CMOS gate that implements:

$$f = ab + cd$$

Your approach will be to use a composition of a single gate that implements $\overline{f}$ followed by an inverter.

(a) Show your circuit diagram for f.

Static CMOS Gates (SP 21)

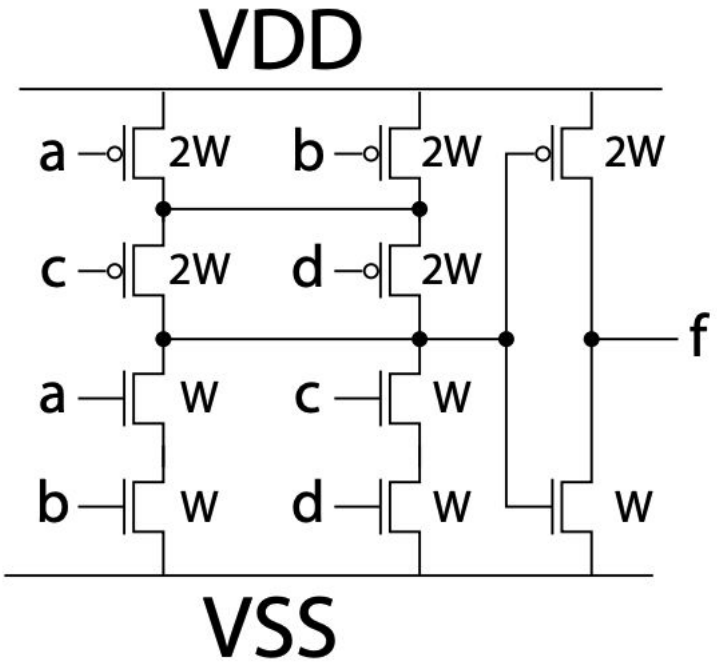


Static CMOS Gates (SP 21)

(b) Size the transistors in your $\overline{f}$ gate so that each input has the same capacitance as a unit sized inverter, and derive the equation for worst case delay. Assume that the resistance per unit width for pFETs is twice that of nFETs. Also size the transistors so that the rise and fall times are equivalent.

This (transistor sizing) is out of scope

Static CMOS Gates (SP 21)



Static CMOS Gates (SP 21)

(c) Now, assuming that your output inverter is unit sized, derive a delay equation for the composite gate.

It will be given that the unit sized inverter has

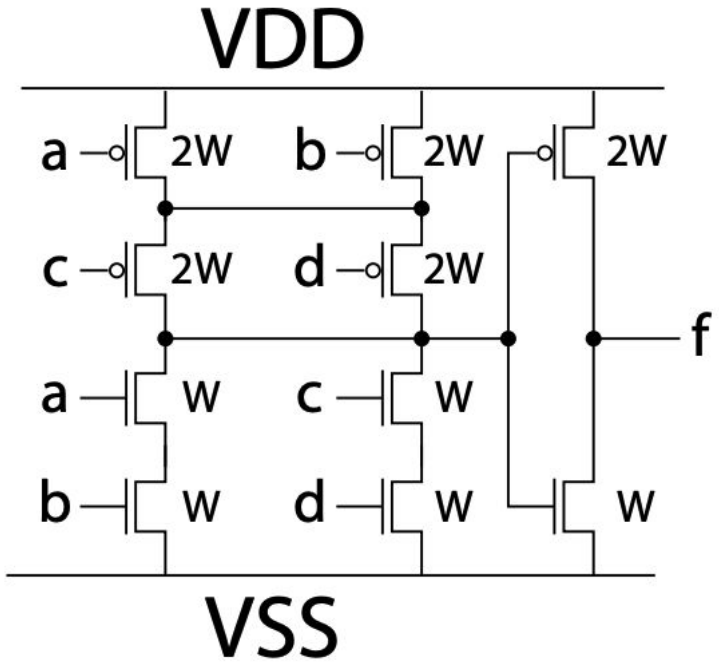
- resistance R_N/W
- input capacitance $3WC_G$
- parasitic capacitance $3W\gamma C_G$

Remember in this problem PMOS has 2x resistance than NMOS

Static CMOS Gates (SP 21)

Your gate:

- resistance $2R_N/W$
- input capacitance $3WC_G$
- parasitic capacitance $6W\gamma C_G$



Static CMOS Gates (SP 21)

$$t_{p,inv} = t_{p0}\left(1 + \frac{f}{\gamma}\right)$$ where $t_{p0} = 0.69\, R_N\, 3\gamma C_G$

$$\begin{aligned}
t_{p,\overline{f}} &= 0.69\left(\frac{2R_N}{W}\right)(C_{int} + C_L) \\
&= 0.69\left(\frac{2R_N}{W}\right)(6W\gamma C_G + C_L) \\
&= 0.69\left(\frac{2R_N}{W}\right)(3W\gamma C_G)\left(2 + \frac{C_L}{3W\gamma C_G}\right) \\
&= t_{p0}2\left(2 + \frac{C_L}{3W\gamma C_G}\right) \\
&= t_{p0}\left(4 + \frac{2C_L}{3W\gamma C_G}\right) \\
&= t_{p0}\left(4 + \frac{2f}{\gamma}\right)
\end{aligned}$$

Because f for your gate is 1
(input capacitances are both $3WC_G$)

$$t_{p,\overline{f}} = t_{p0}\left(4 + \frac{2}{\gamma}\right)$$

By taking the sum of delays

$$t_p = t_{p0}\left(5 + \frac{2}{\gamma} + \frac{f}{\gamma}\right)$$

where f is ratio of load capacitance over input capacitance of unit inverter

Static CMOS Gates (SP 21)

(d) You realize that you might be able to scale up the size of the output inverter for better performance—a 4X inverter seems like a good choice. Derive a delay equation for this new composite gate.

Static CMOS Gates (SP 21)

$$t_{p,\overline{f}} = t_{p0}\left(4 + \frac{2f}{\gamma}\right)$$

Now inverter is 4x larger, f = 4.

$$t_{p,\overline{f}} = t_{p0}\left(4 + \frac{8}{\gamma}\right)$$

Then total delay is

$$t_p = t_{p0}\left(5 + \frac{8}{\gamma} + \frac{f}{\gamma}\right)$$

FSMs and State Encoding (SP 21)

Some particular sequential circuit has a 3-bit output labeled $[x_2, x_1, x_0]$. It outputs a new value on each clock cycle in the following repeating sequence:

`3, 2, 5, 7, 6, 1, 4, 3, 2, ...`

Using flip-flops and 2-input ANDs and ORs, and, if needed, inverters. Derive a circuit with this behavior. Optimize for cost by trying to minimize the number of logic gates. Show your work. *Hint: think about this as a FSM.*

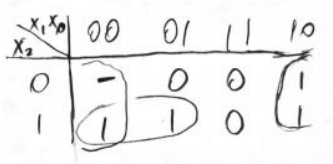
FSMs and State Encoding (SP 21)

In binary, the sequence, encoded as $\{x_2, x_1, x_0\}$, is 011, 010, 101, 111, 110, 001, 100, 011, 010.

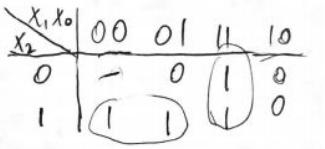
Let x be output and y be input of the FFs.

x2	x1	x0	y2	y1	y0
0	0	0	-	-	-
0	0	1	1	0	0
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	0	1	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	1	1	1	0

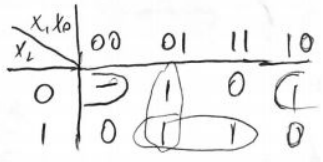
y0



y1



y2

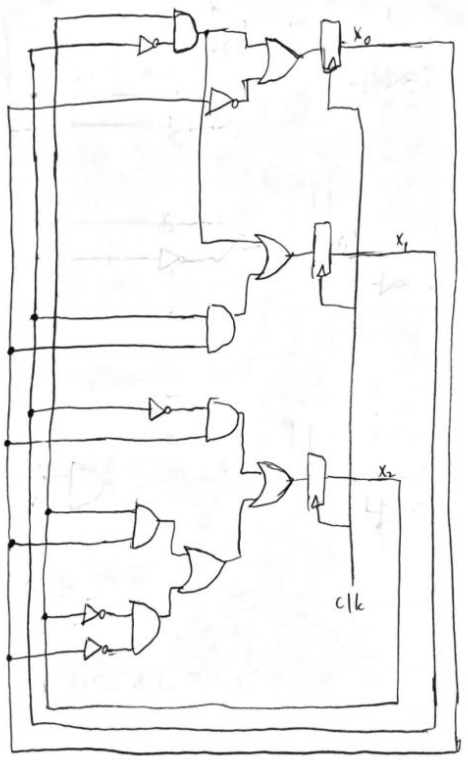


FSMs and State Encoding (SP 21)

y0 $= x_2\bar{x}_1 + \bar{x}_0$

y1 $= x_2\bar{x}_1 + x_1x_0$

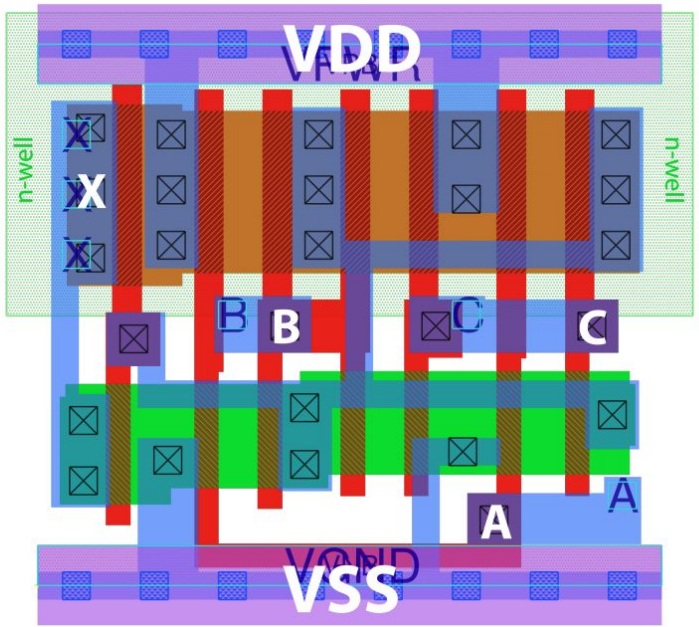
y2 $= \bar{x}_1x_0 + x_2x_0 + \bar{x}_2\bar{x}_0$



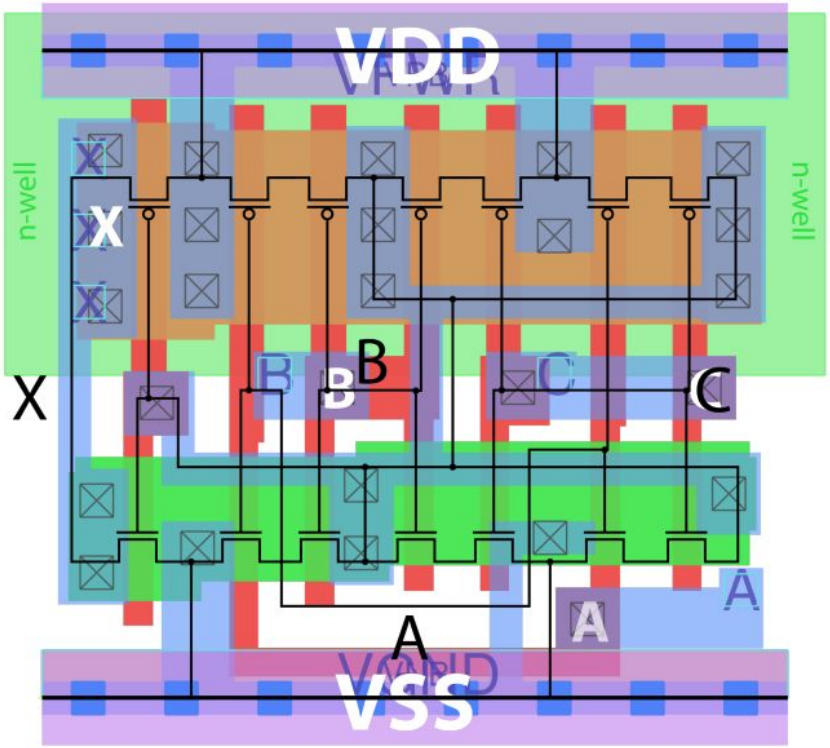
Layout (SP 21)

Consider the layout shown below.

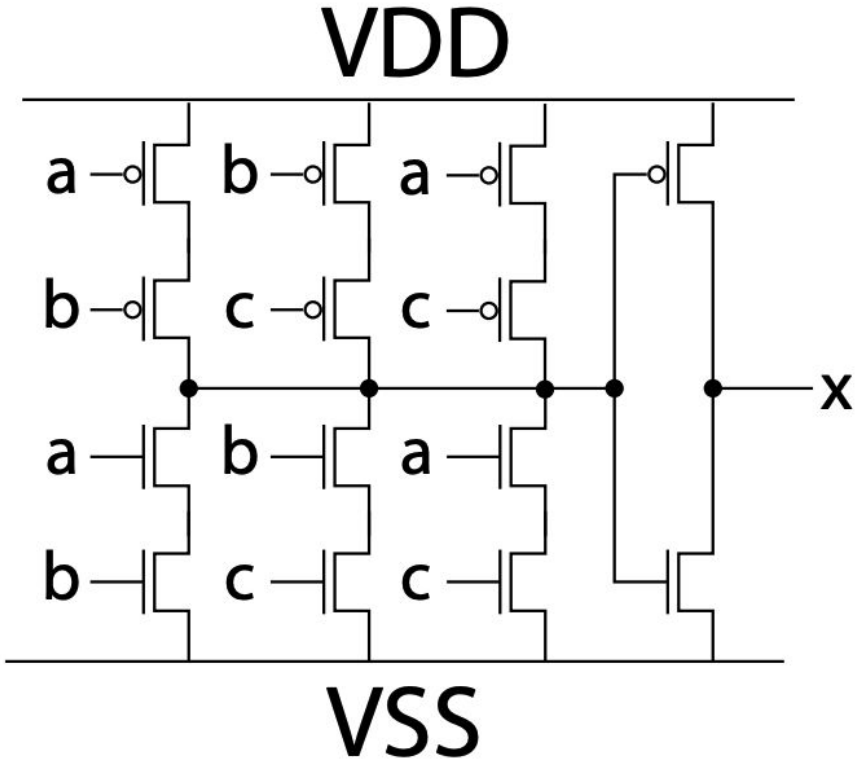
(a) Extract the transistor level circuit diagram and sketch it.
(b) Write an Boolean expression for its function.
(c) Is there a common name for this function?



Layout (SP 21)



Layout (SP 21)



Layout (SP 21)

Majority vote:

$$x = ab + ac + bc$$