EECS 151 Disc 6

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Contents

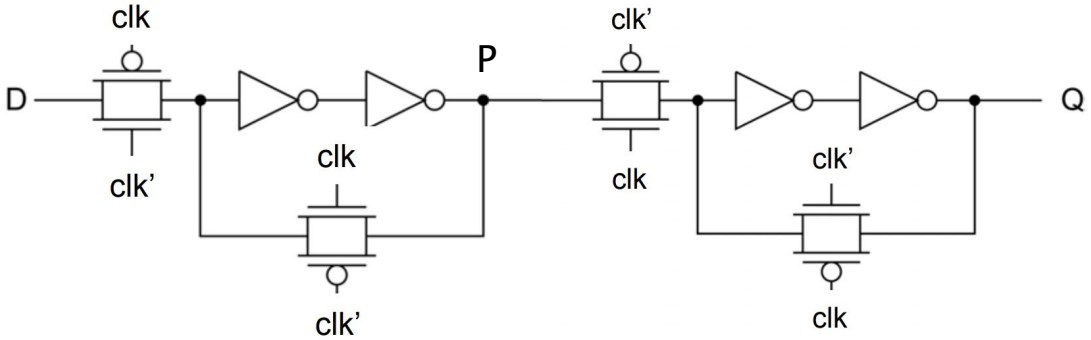
- FF Timing
- Retiming
- Gate Sizing (Inverter Chain)
- Elmore Delay
- Rebuffering
- Transistor Sizing (SPICE Simulation)

Flip-Flops

Setup time: Time needed for D to overwrite the first loop

Clk-q delay: The signal needs to pass some transistors from P to Q

Hold time: Clock signal might arrive late, so D needs to be stable a little longer

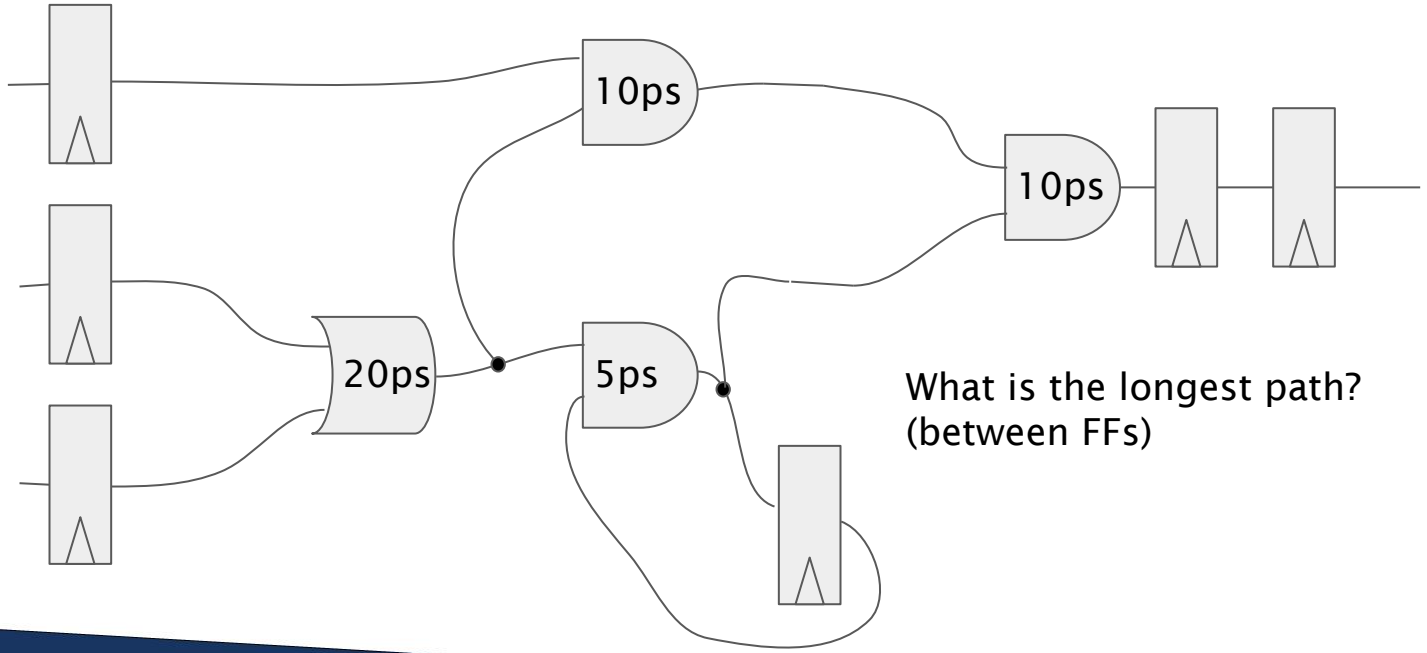


Retiming

Clock period >= clk-q delay + critical path delay + setup time

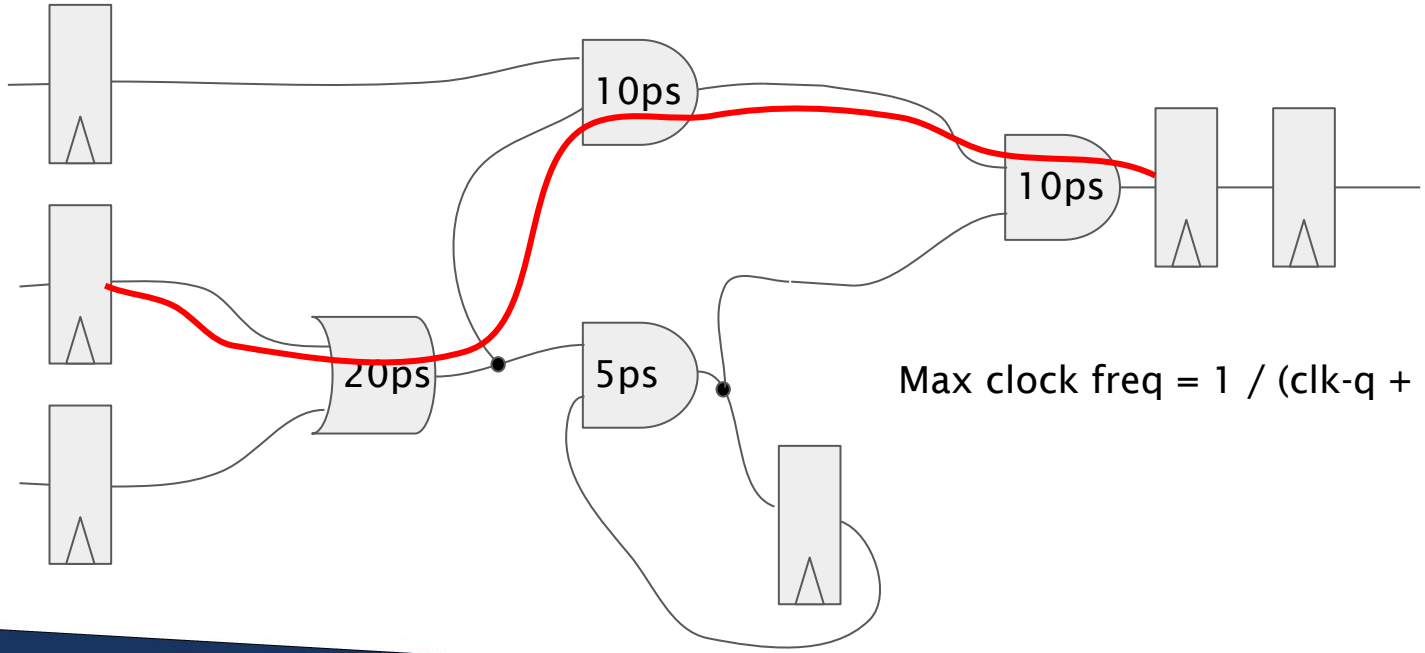
(Hold time is important when it is larger than clk-q delay, where the next cycle signal may arrive too fast. We need some buffers to delay the signal in that case.)

Example: Retiming



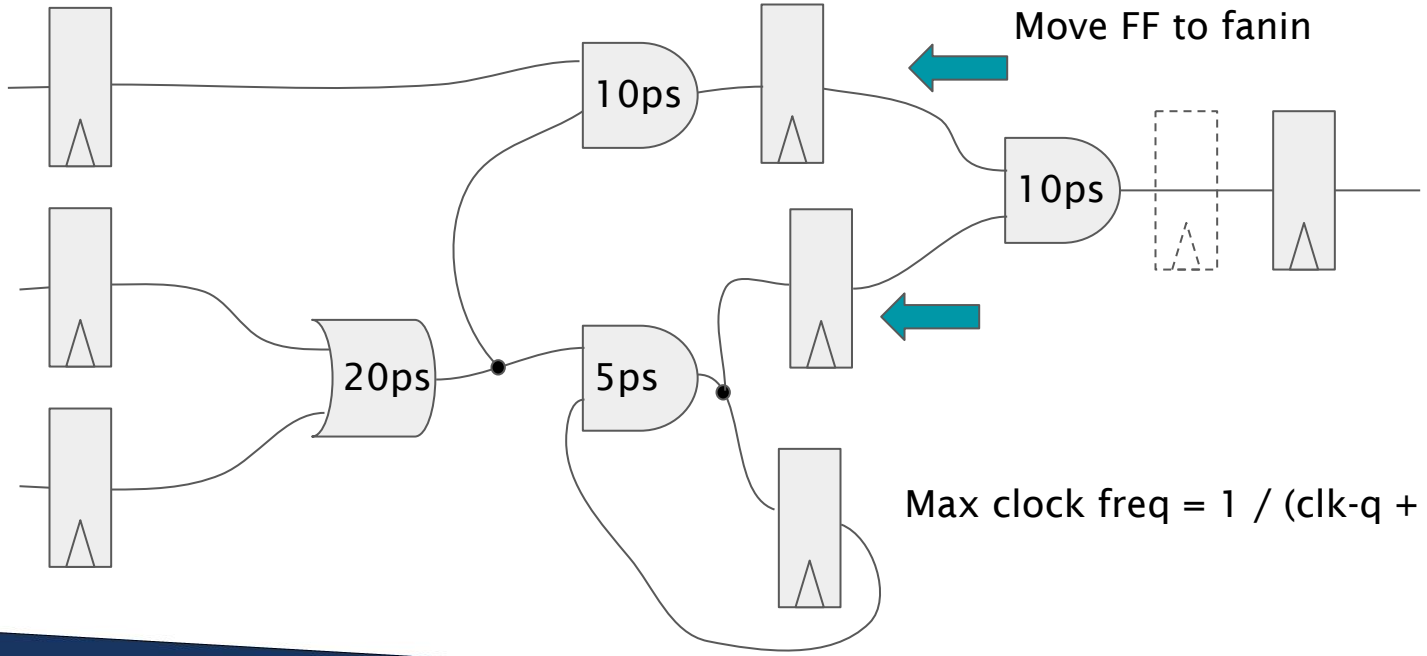
What is the longest path?
(between FFs)

Example: Retiming



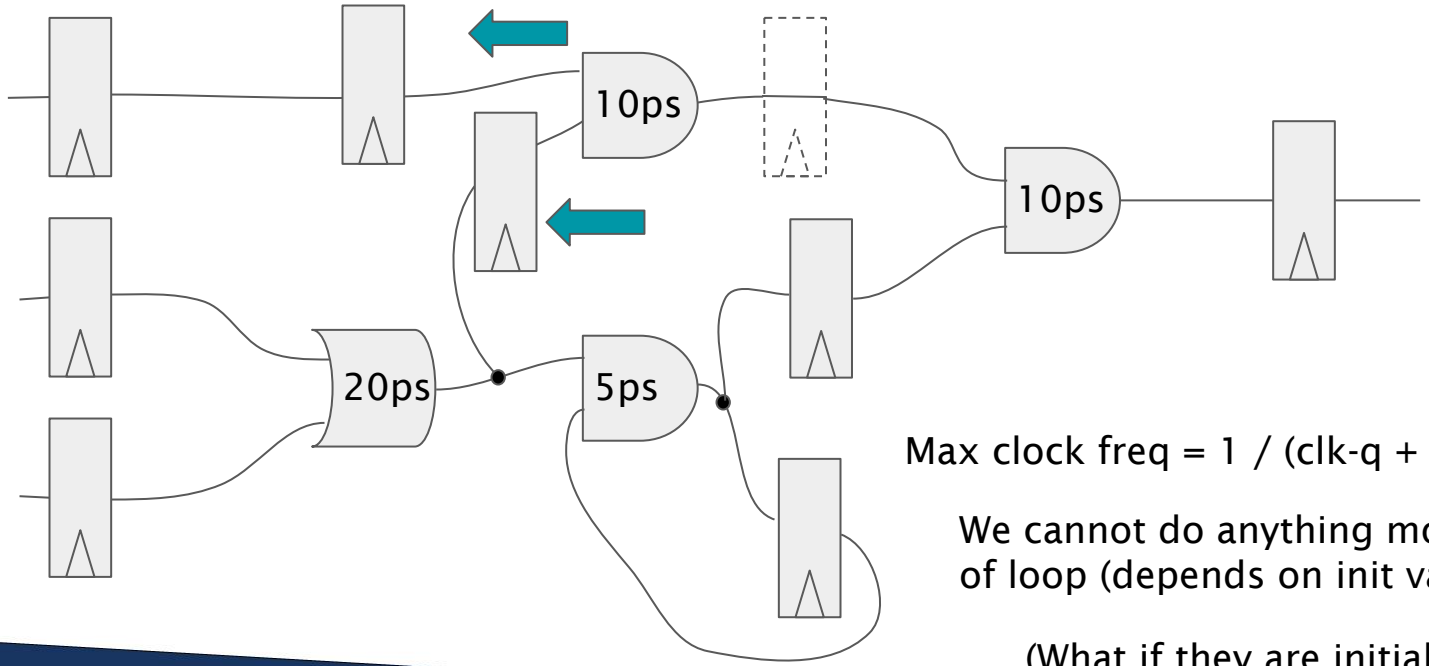
Max clock freq = 1 / (clk-q + setup + 40ps)

Example: Retiming



Example: Retiming

Move FF to fanin



Max clock freq = 1 / (clk-q + setup + 25ps)

We cannot do anything more because of loop (depends on init values of FFs)

(What if they are initialized to 0?)

Gate Sizing

Driving a large capacitor with a small gate is slow.

Driving a large capacitor with a large gate is fast… but then we also need to drive the large gate.

Inverter Chain

Solution: use N stages. How many?

- Large N: delay dominated by accumulation of delay from each stage
- Small N: delay dominated by slow capacitor charging.

Optimal N is somewhere in the middle.

Example: Inverter Chain

Design an inverter chain to drive a 512 fF load capacitor.

First stage has 2fF input capacitance.

Assume:

- Gamma = 1.5, optimal fanout is 4

$$t_p = N \cdot t_{p0}(1 + \sqrt[N]{F}/\gamma)$$

$$\gamma + \sqrt[N]{F} - \frac{\sqrt[N]{F}\, lnF}{N} = 0$$

$$f = e^{(1+\gamma/f)} \qquad f = \sqrt[N]{F}$$

Solution: Inverter Chain

Design an inverter chain to drive a 512 fF load capacitor.

First stage has 2fF input capacitance.

$$f = \sqrt[N]{F}$$

$$4 = \sqrt[N]{(512/2)} = \sqrt[N]{256}$$

Gives N = 4, so use 4 inverters.

Elmore Delay

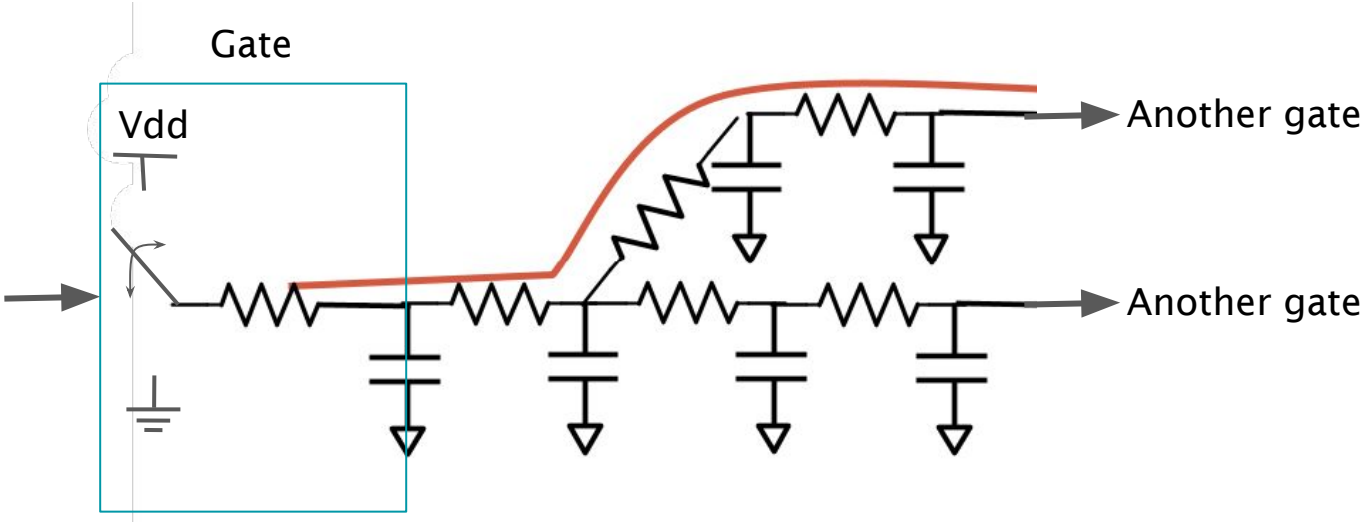
We have only considered delay of gates

Wires also cause some delay, especially in recent technologies

Elmore delay:

- For each resistance on the path, multiply its value by sum of all dependent capacitance
- Sum up all products

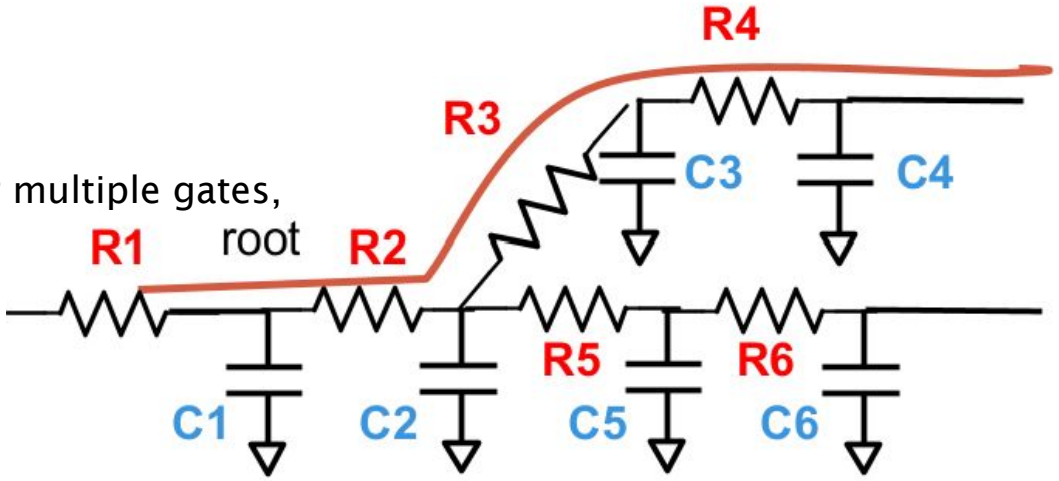
Example: Elmore Delay



Example: Elmore Delay

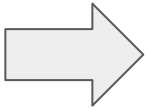
$$\text{Delay} / \ln 2 = R1(C1 + C2 + C3 + C4 + C5 + C6) + R2(C2 + C3 + C4 + C5 + C6) + R3(C3 + C4) + R4(C4)$$

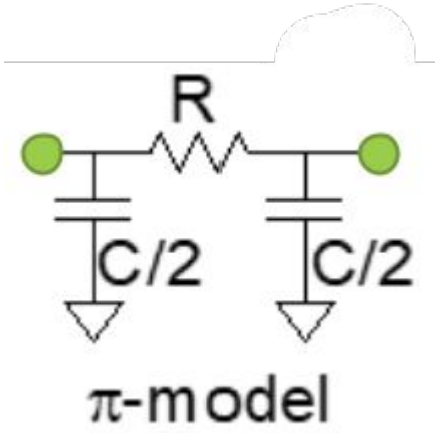
If you are calculating delay over multiple gates, just sum up their delays



Π (PI) model

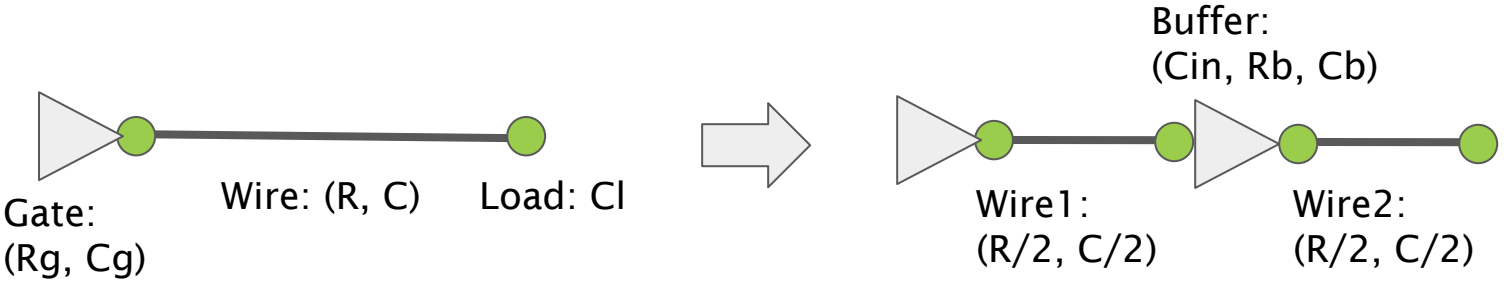
Wire: (R, C)





Rebuffering

Partition a long wire and drive each piece by a new buffer (or inverter)



Delay/ln2 = Rg(Cg+C+Cl) + R(C/2 + Cl)

Delay/ln2 = Rg(Cg + C/2 + Cin) + (R/2)(C/4 + Cin)
+ Rb(Cb + C/2 + Cl) + (R/2)(C/4 + Cl)

Homework: Generalize this to N partitions and find the best N using its derivative

Transistor Sizing

We can reduce delay by adjusting gate sizes

Increasing gate size means increasing size of all transistors inside uniformly

How about relative sizes of transistors in a gate?

Transistor Sizing

Usually PMOS is weaker (more resistance)

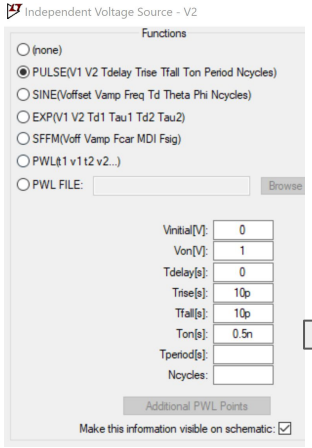
- We need to make them wider than NMOS
- This balances high-to-low and low-to-high delay

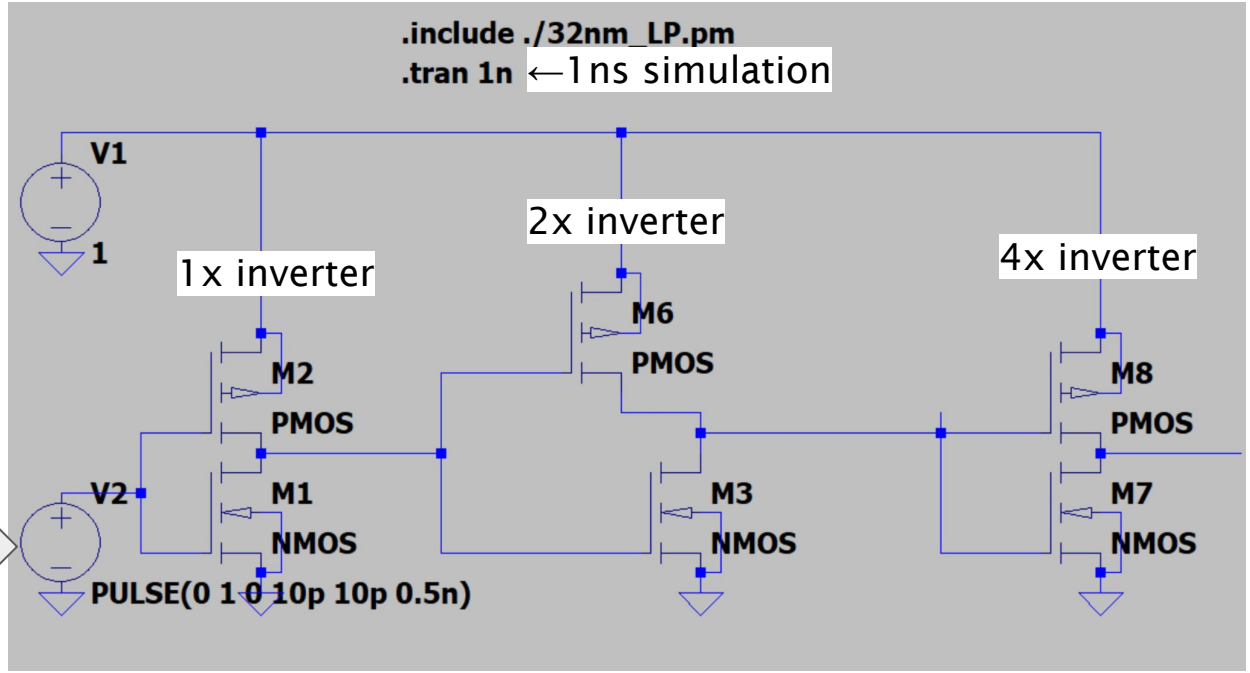
If transistors are connected in a series, their resistance is accumulated

- We need to make them wider than other parallel transistors
- This balances delay for different input patterns

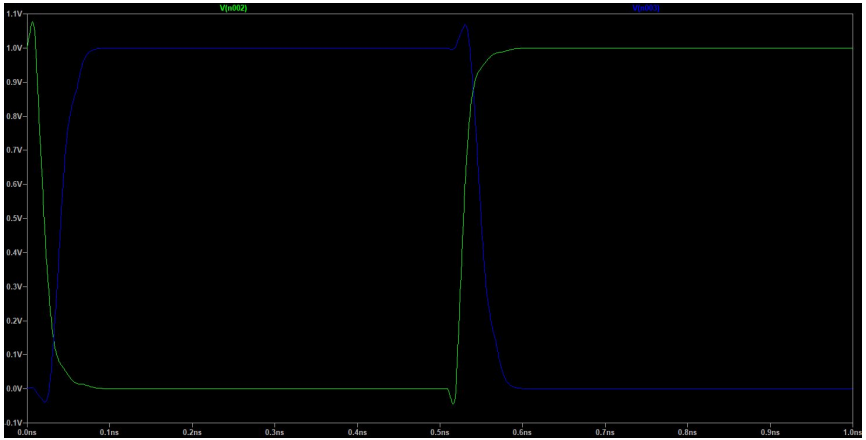
SPICE Simulation

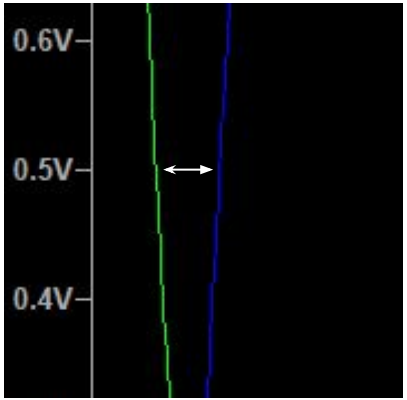
Advanced setting for voltage



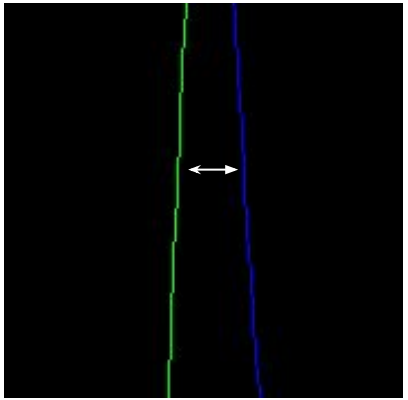


Plot of I/O of the 2nd Inverter





Low-to-high delay

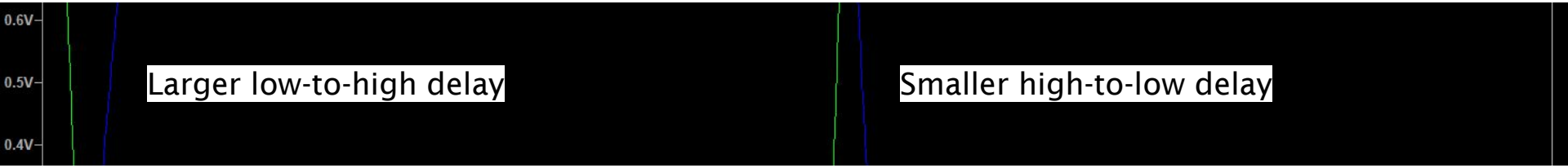


High-to-low delay

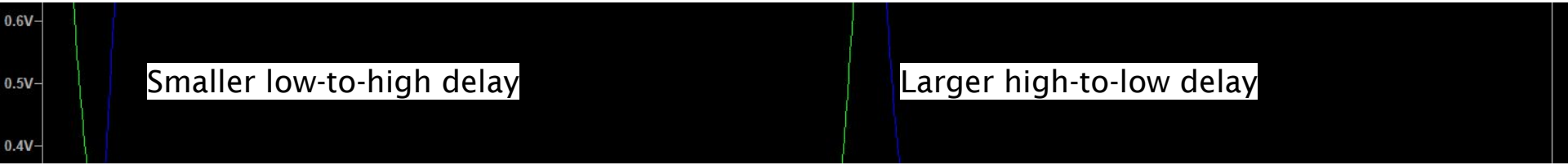
Measure the time between Vdd/2 points

PMOS Sizing

Smaller PMOS:



Larger PMOS:



Why?