

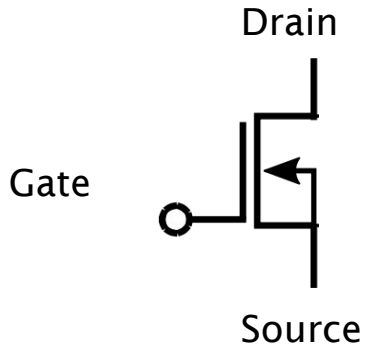
EECS 151 Disc 5

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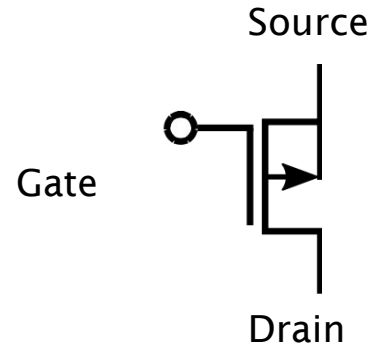
Contents

- MOS Transistors
- Switch Networks
- CMOS
- Layout
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N-MOS and P-MOS

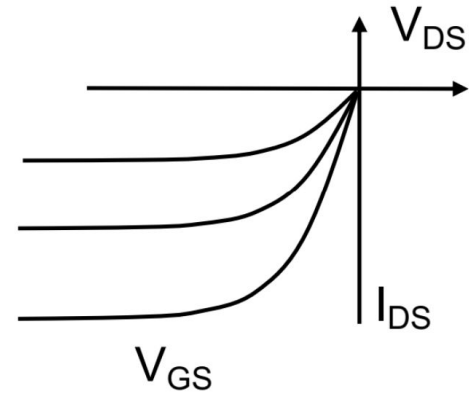
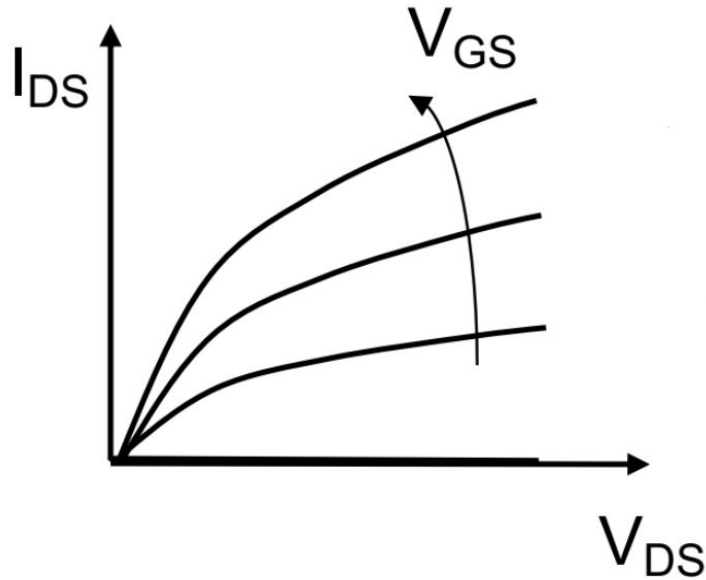


NMOS



PMOS

V-I Characteristics



PMOS works with negative voltages

Note: NMOS is stronger (more current) than PMOS. Wider is stronger.

More SPICE Simulation

```
.param your_param 0  
.step param your_param 1 9 2
```

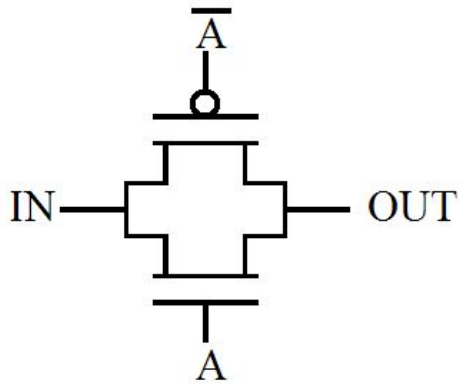
Plots each case ($\text{your_param} = 1, 3, 5, 7, 9$) with different colors

Can be combined with `.dc` to plot multiple curves

Transmission Gate

NMOS is bad at passing 1; PMOS is bad at passing 0 (why?)

Transmission gate:

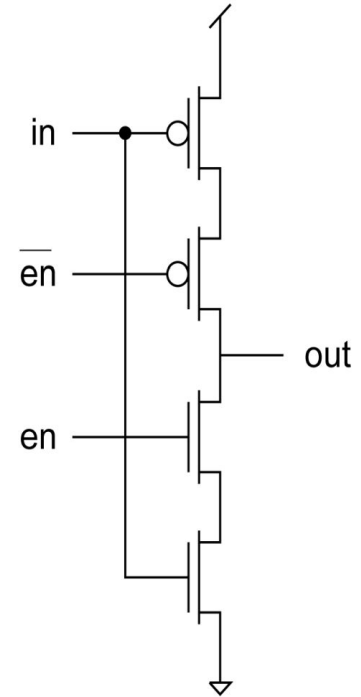


Tri-state Buffer

Transmission gates do not provide power, accumulating a load on the driver

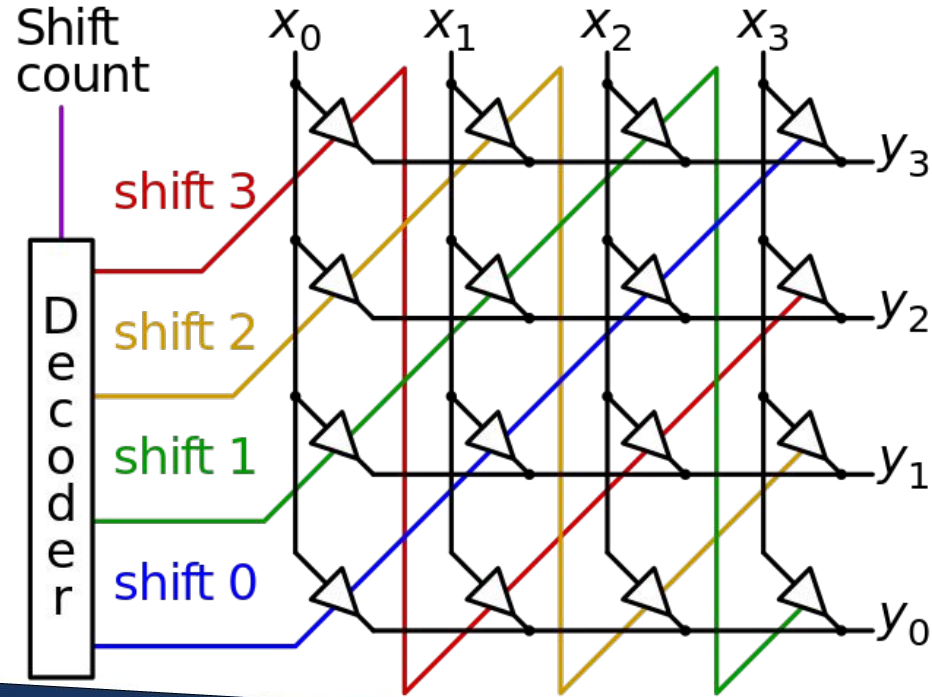
Alternative: Tri-state buffers

- Pass input to output if enabled
- Oneway
- Use a new power supply (VDD, GND)



Tri-state buffer with inverted output

Barrel Shifter



CMOS Logic

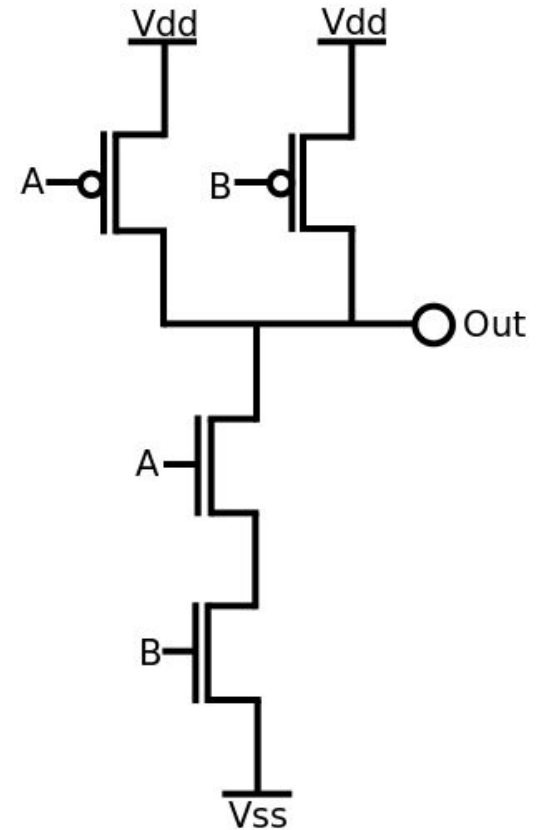
The majority of digital logic is implemented using CMOS.

- Pull-up networks : PMOS and VDD
- Pull-down networks : NMOS and GND

NAND2 Gate

Show why this is a NAND gate in two ways:

- By analyzing the PDN
- By analyzing the PUN

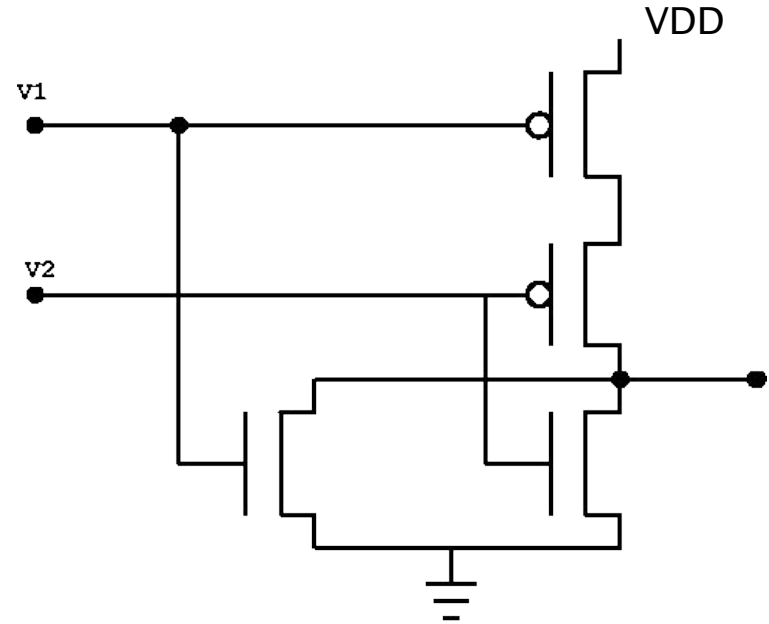


NOR₂ Gate

Draw a CMOS NOR₂ gate.

NOR₂ Gate

Draw a CMOS NOR₂ gate.



AND-OR-Invert (AOI) Gate

Draw a complex CMOS gate implementing a 2-1 AOI:

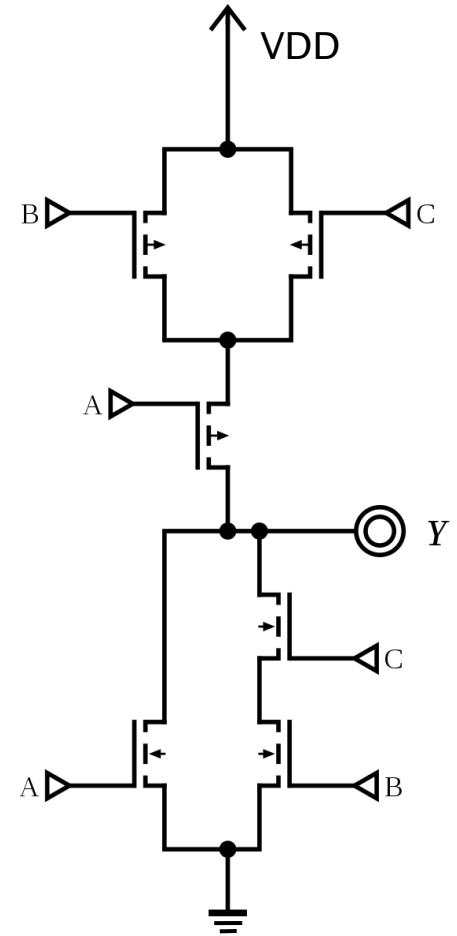
$$Y = (A + B C)'$$

(Hint: Complement the function for PDN)

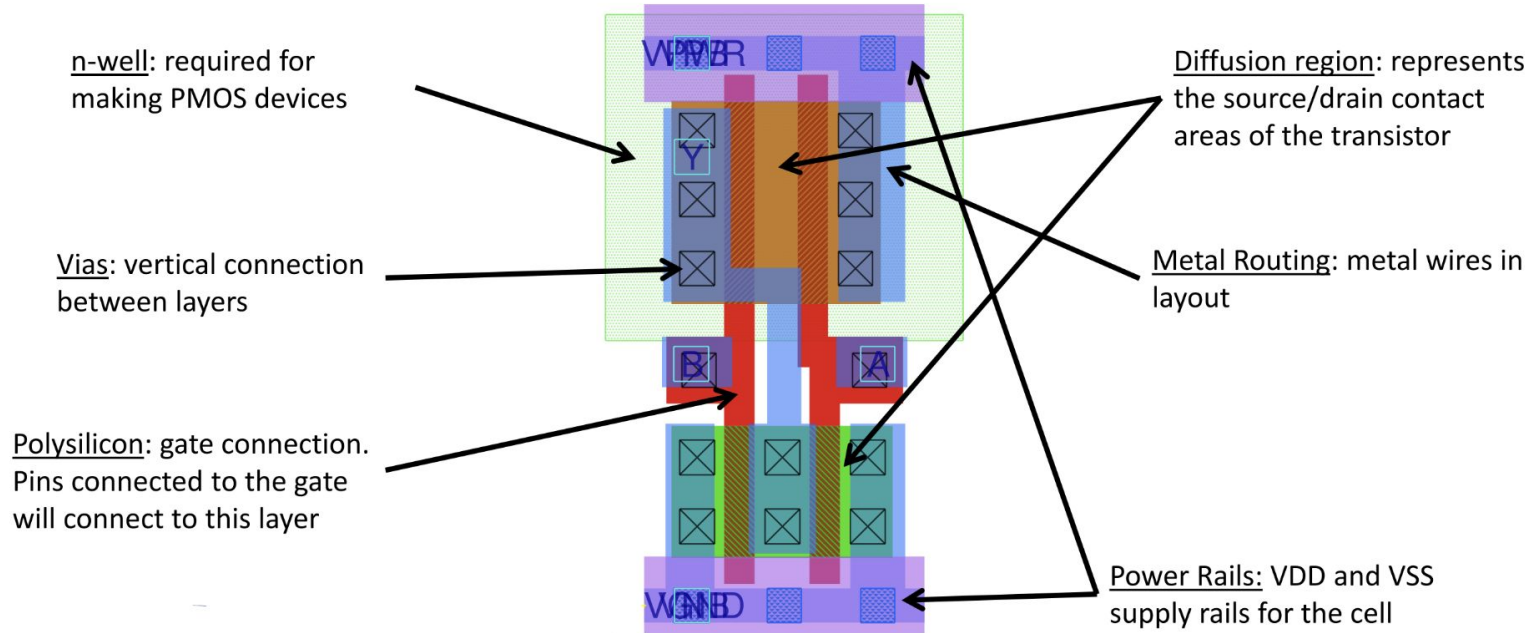
AND-OR-Invert (AOI) Gate

$$Y = (A + B C)' = A' (B' + C')$$

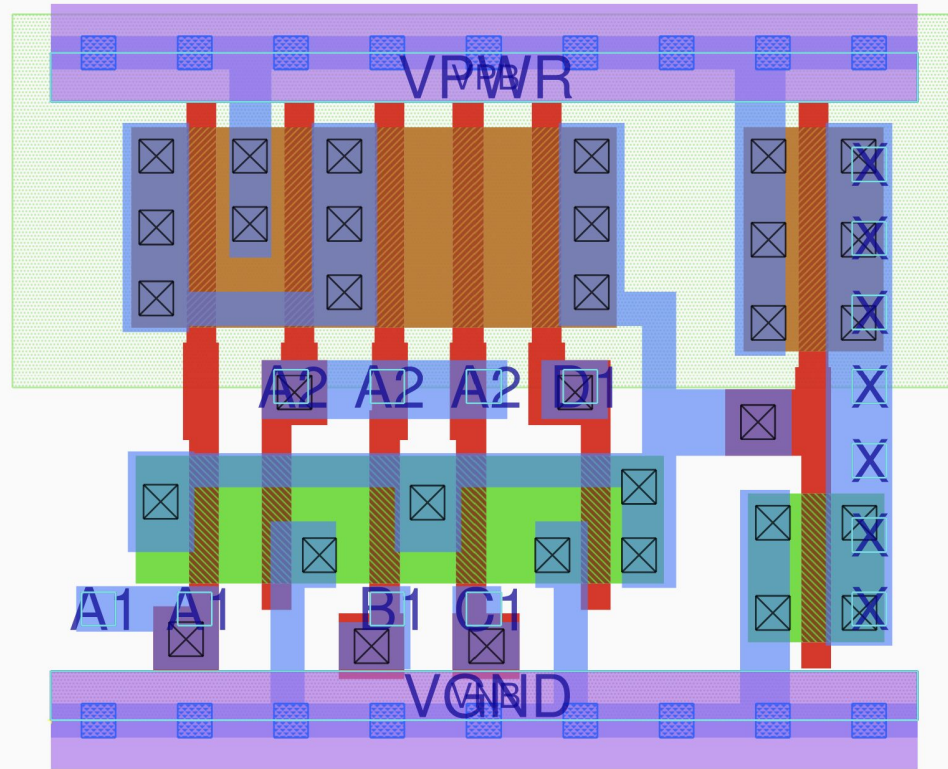
$$Y' = A + B C$$

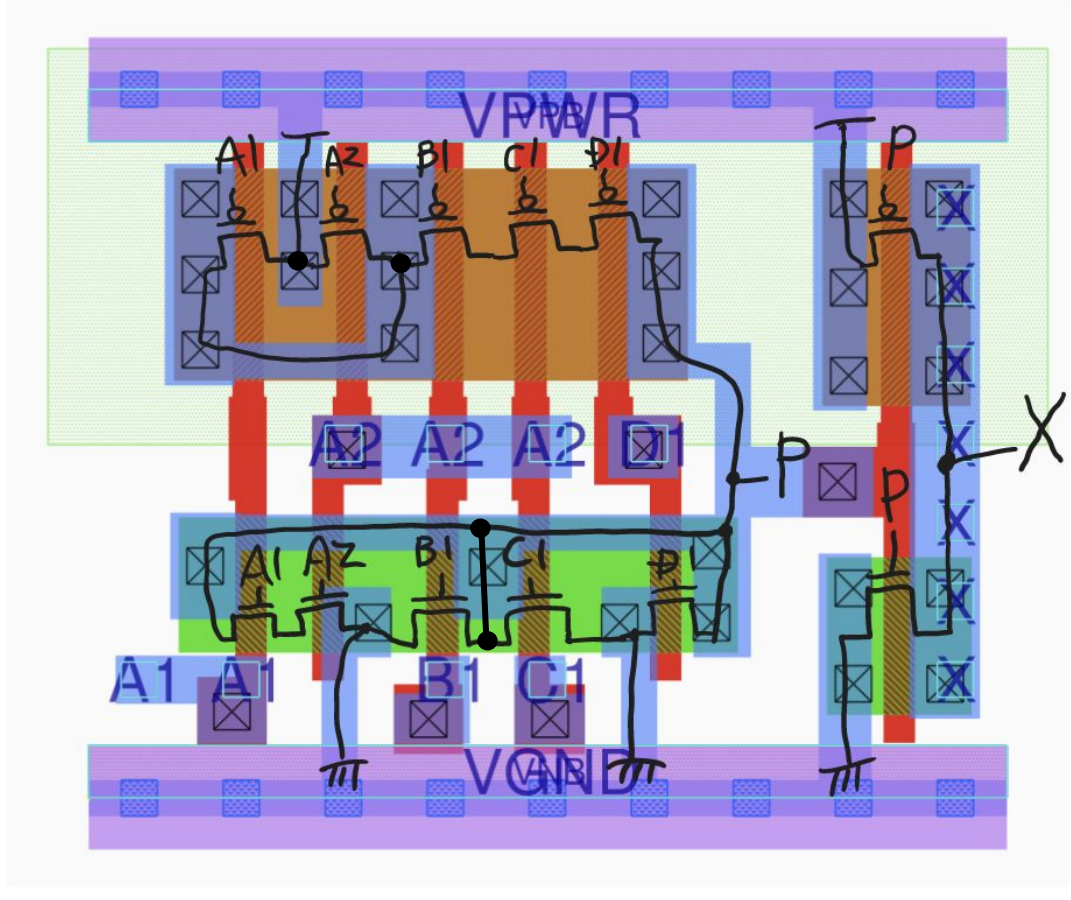


Layout

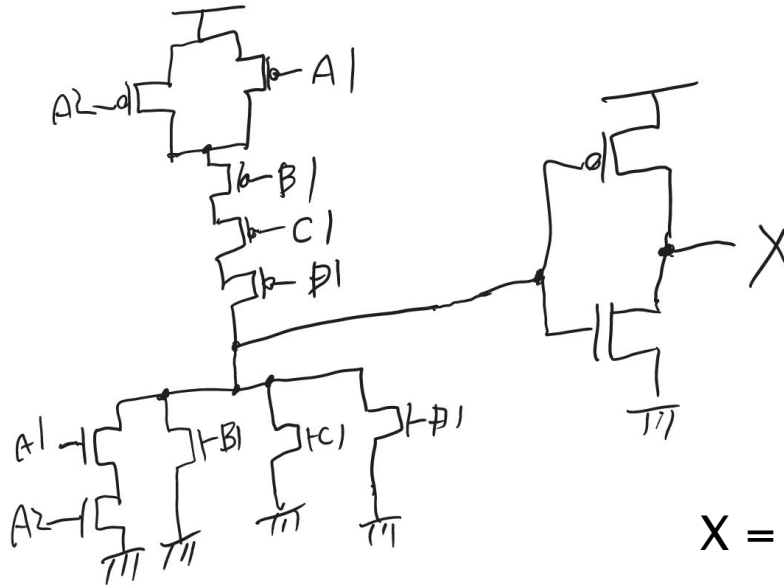


Example



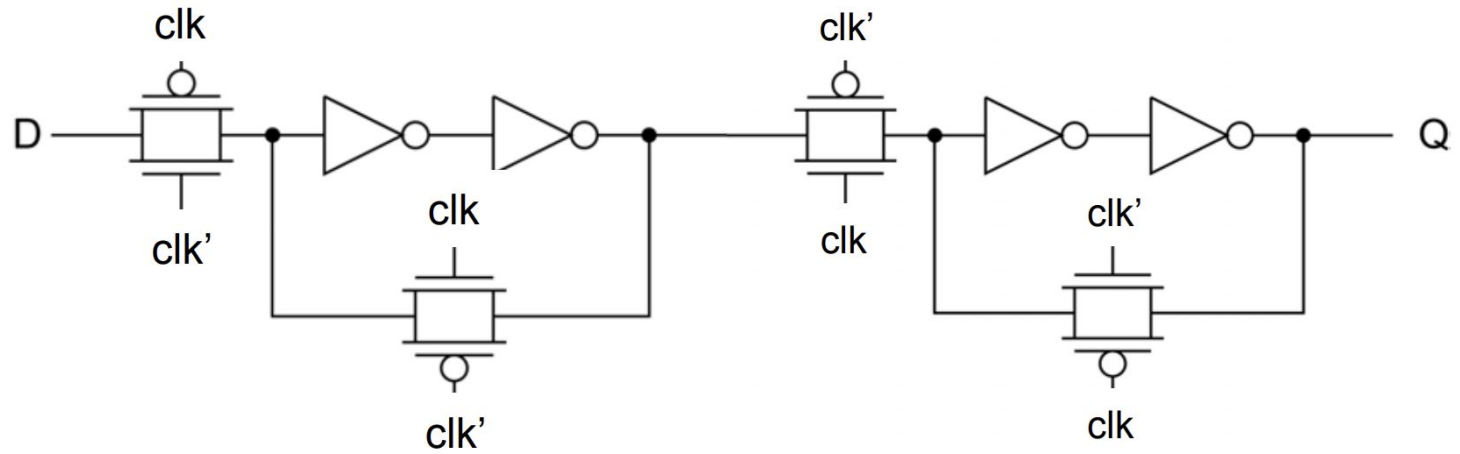


Transistor-Level Schematic



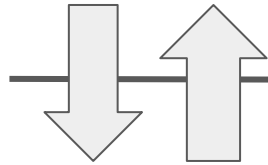
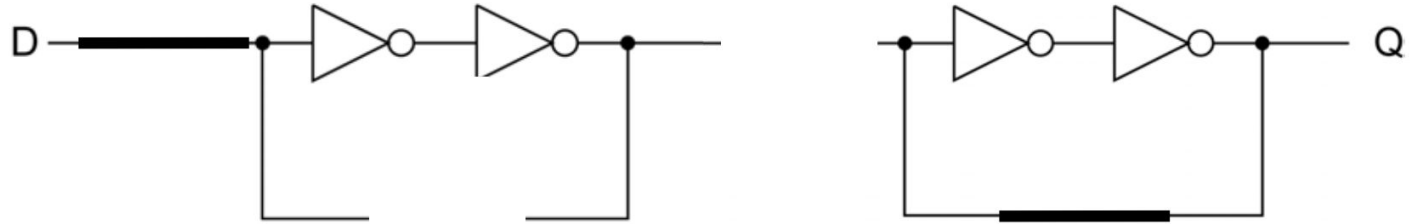
$$X = A1 A2 + B1 + C1 + D1$$

Flip-Flops



Flip-Flops

clk=0



clk=1

