EECS 151 Disc 12

Rahul Kumar (session 1)
Yukio Miyasaka (session 2)

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Contents

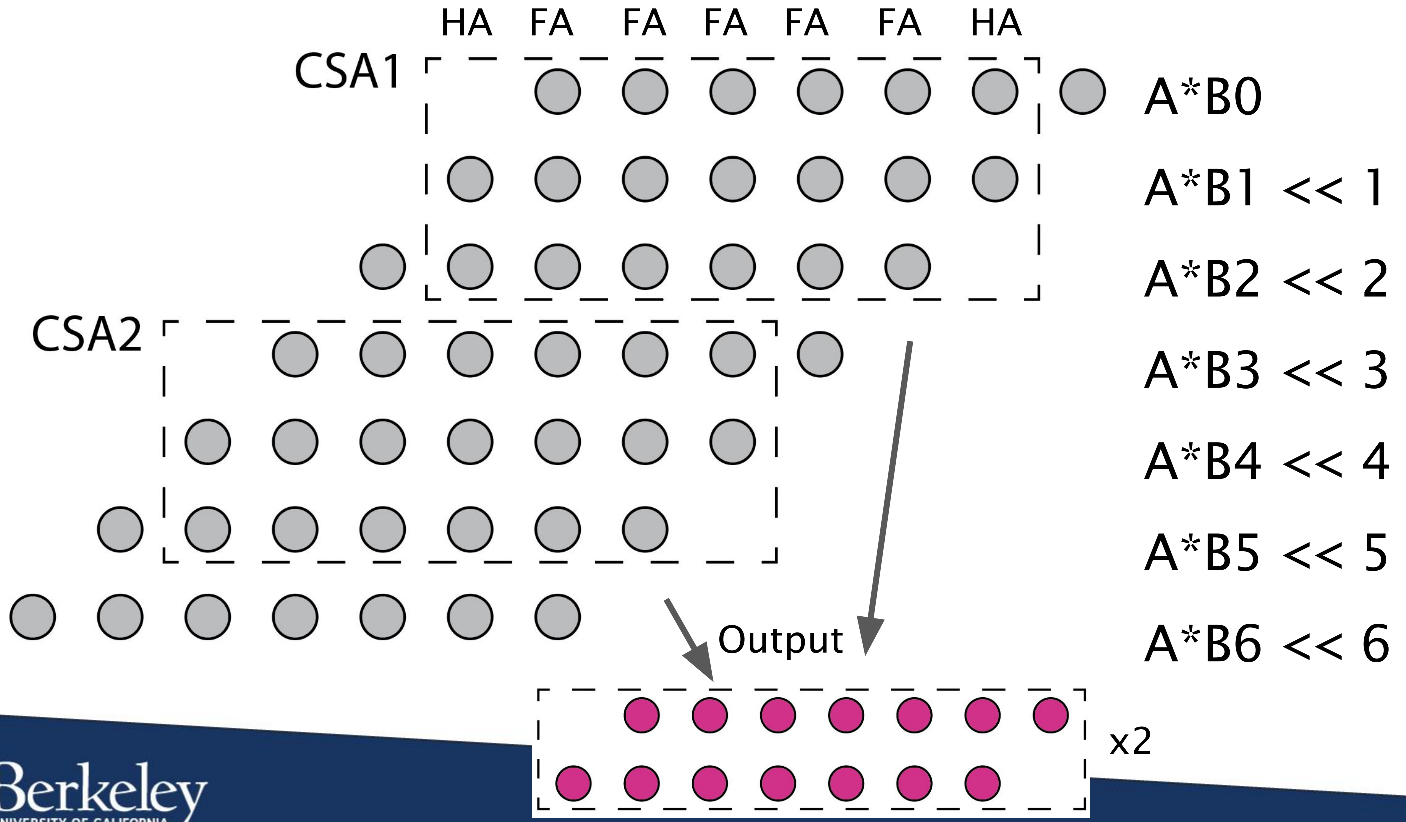
- Wallace tree
- Signed multiplication
- Multiplication by a constant
- Clocks
- Packaging

Announcement

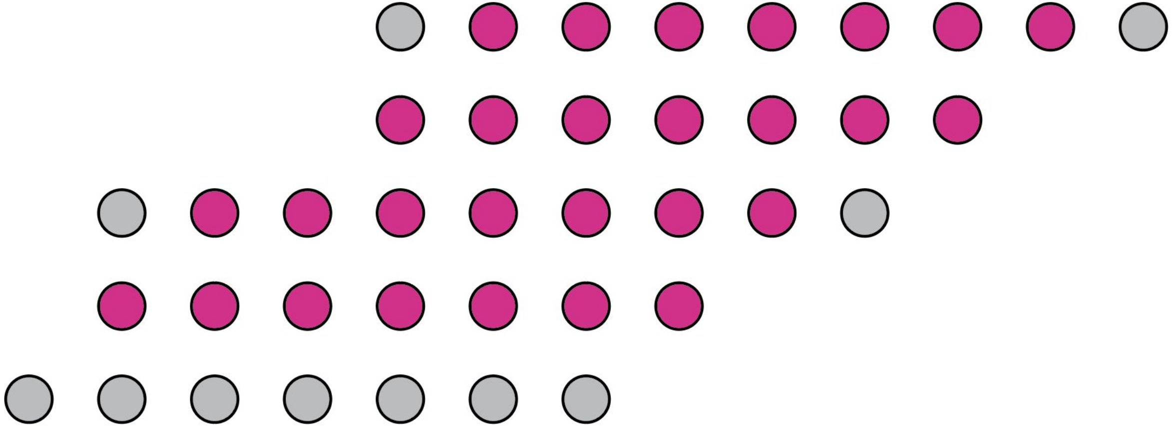
- HW11 is not as short as we expected
- However, each problem is quite simple (~5 min)
- Due May 8 Monday, solution will be posted just after deadline

- Unfortunately, we don't have time to do review for the final

7x7 Wallace Tree (Unsigned Multiplier)

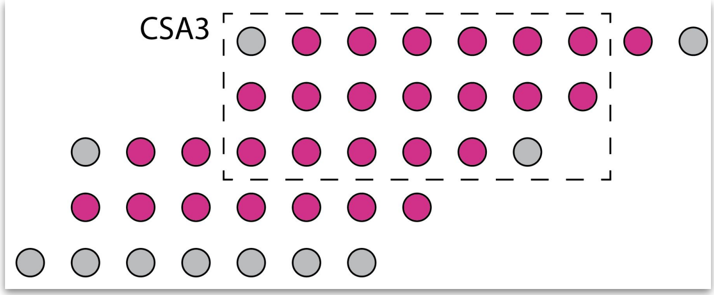


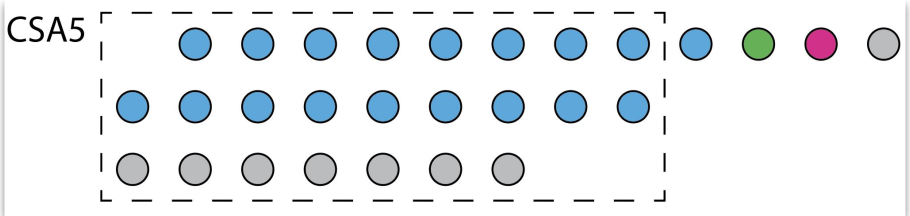
7x7 Wallace Tree: After 1st Stage

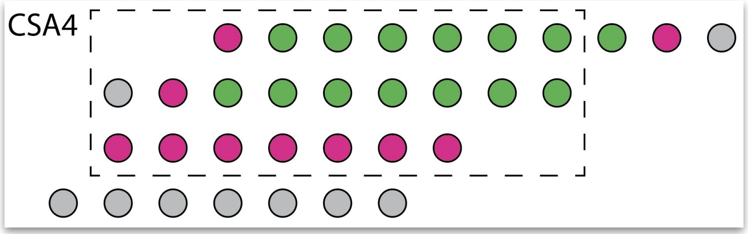


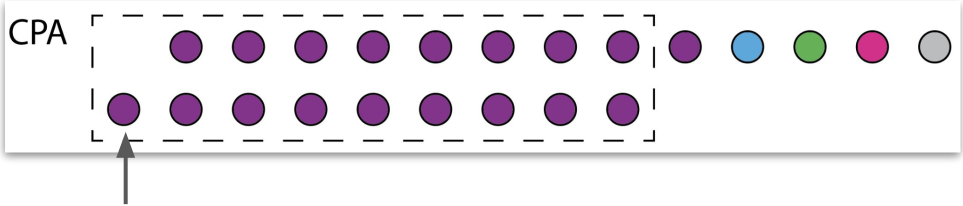
7x7 Wallace Tree: Following Stages

(There were some bugs in last week's slide)









The MSB adder can be just an XOR, since the result of 7x7 does not exceed 14 bits.

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Signed Multiplication

B = {b3, b2, b1, b0} = b0 + (2*b1) + (4*b2) - (8*b3)

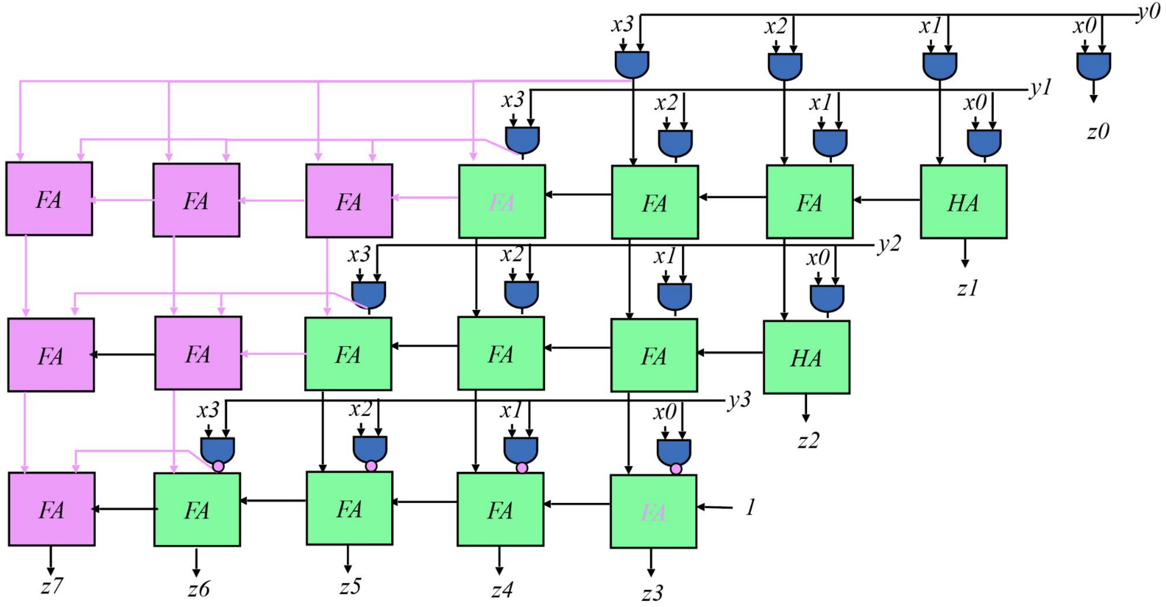
A*B = A*b0 + A*(2*b1) +A*(4*b2) - A*(8*b3)

= A*b0 + (A<<1)*b1 + (A<<2)*b2 - (A<<3)*b3

- One more left shift each time
- Subtract the partial product for the MSB of B
- Sign extend partial products properly (2N is safe, but you can save a little by using some techniques)

Straightforward Signed Multiplier

```
                                         X3    X2    X1    X0
                                     *   Y3    Y2    Y1    Y0
                                     --------------------
  X3Y0  X3Y0  X3Y0  X3Y0  X3Y0  X2Y0  X1Y0  X0Y0
+ X3Y1  X3Y1  X3Y1  X3Y1  X2Y1  X1Y1  X0Y1
+ X3Y2  X3Y2  X3Y2  X2Y2  X1Y2  X0Y2
- X3Y3  X3Y3  X2Y3  X1Y3  X0Y3
-----------------------------------------
    Z7    Z6    Z5    Z4    Z3    Z2    Z1    Z0
```

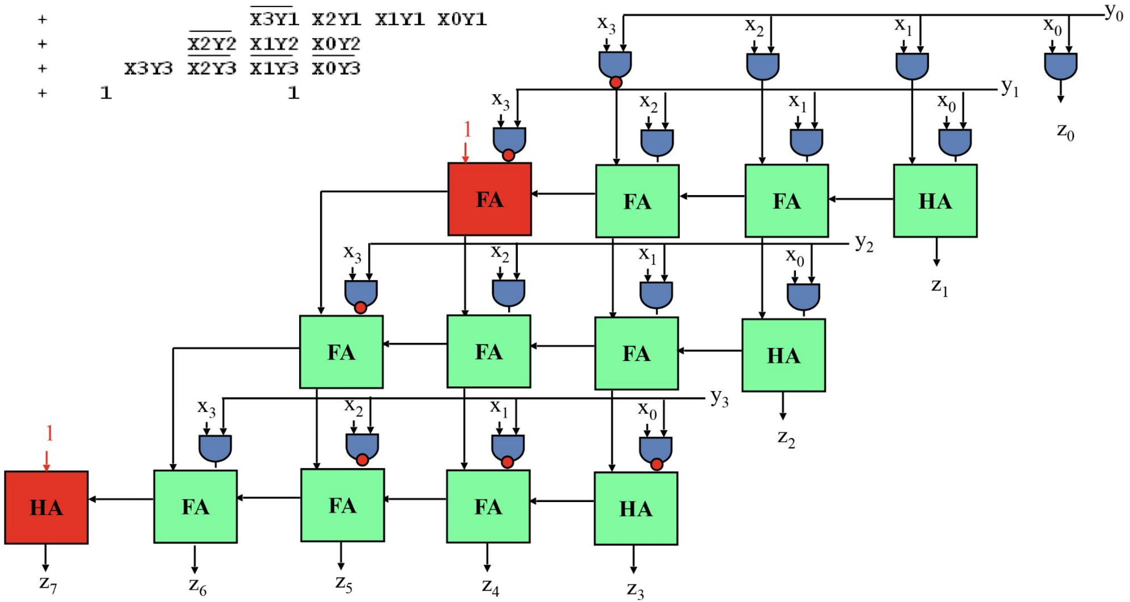


Baugh-Wooley's Algorithm

- Replace sign extension with negation and minus one at the MSB
  - aa…axyz = a'xyz - 1000 because
    - 00…0xyz = 1xyz - 1000
    - 11…1xyz = 0xyz +11…1000 = 0xyz - 1000
- Also apply 2's complement to the last partial product
  - -aaxyz = a'a'x'y'z' + 1 = ax'y'z' - 1000 + 1
- Precompute constants
  - -1000 - 10000 - 100000 - 1000000 + 1000 = -1110000 = +10010000

Baugh-Wooley's Signed Multiplier

					$\overline{X3Y0}$	X2Y0	X1Y0	X0Y0
+				$\overline{X3Y1}$	X2Y1	X1Y1	X0Y1	
+			$\overline{X2Y2}$	X1Y2	X0Y2			
+		X3Y3	$\overline{X2Y3}$	$\overline{X1Y3}$	$\overline{X0Y3}$			
+	1			1				



Multiplication by a Constant

- Multiplication by a constant is just shift-and-add
  - 75X = 1001011X = (X << 6) + (X << 3) + (X << 1) + X
- CSD representation utilizes subtraction
  - 01…11 to 10…01’ (1’ here means minus one)
  - 11’ to 01, and 1’1 to 01’
    - 75 = 1001011 = 1001101’ = 10101’01’
    - 75X = (X << 6) + (X << 4) - (X << 2) - X
    - Doesn’t help in this case

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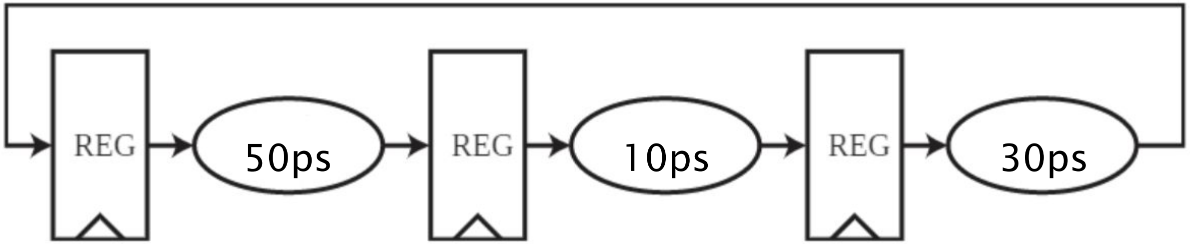
Constant Coefficient Multiplication

- Break down the constant and cascade shift-and-add
- 75 = 3*5*5
  - (3 * 25): 3 is (2+1) and 25 is (16+8+1) -> 3 adders
  - (5 * 15): 5 is (4+1) and 15 is (16-1) -> 2 adders (one used as a subtractor)
- Y = (X << 2) + X
- Z = (Y << 4) - Y
- Then, Z = 75X

Clock Skew

- Clock skew … adjust delay of clock signal to reduce max delay



+a ps

(50 - a) ps

(10 + a) ps

Each stage has 30ps delay when a = 20.

Hold Time Constraint

Near the end of cycle:

And if delay of logic is too small:

If R1 is triggered first:

R2 cannot fetch 0 correctly:

Clock Constraints

- Setup time constraint
  - T > clock_to_q + setup + max_delay + 2*jitter
- Hold time constraint
  - clock_to_q + min_delay > hold + 2*jitter

Packaging

- C4 (solder balls) works better (smaller R) than bond wires
- Still, need to consider inductive effects
    - V_diff = L * dI/dt should be less than 0.1V
- Decoupling capacitors makes current spike smoother (low pass)
- ESD protection using diodes