EECS 151/251A Midterm 1 Information

Exam Date: Mar 14$^{\text{th}}$, 2019

The exam will take place Thursday March 14, 6–9PM in 306 Soda Hall. The exam comprises a set of questions with 1 point per expected minute of completion with a total of approximately 90 points. 251A students will be asked to complete extra questions. All students are allowed one 2-sided 8.5×11 inch sheet of notes. No calculators, phones, or other electronic devices will be allowed. Slide-rules will be permitted.

Topics:

1. Moore's Law Definition and Consequences
2. Dennard Scaling and Consequences
3. Cost/Performance/Power Design Tradeoffs and Pareto Optimality
4. Definitions and representations of combinational logic
5. Principle of restoration
6. Basic principle behind edge-triggered clocking and RTL design methodology
7. Digital system implementation technology alternatives and relative strengths and weaknesses
8. FPGA versus ASIC cost analysis
9. Principle behind structural versus behavioral hardware description
10. Basic Verilog descriptions for combinational logic
11. Verilog generators blocks
12. Verilog inference of state elements
13. FPGA reconfigurable fabric architecture
14. Details of FPGA fabric interconnect switches
15. Details of FPGA logic blocks with LUT

16. Logic circuit partitioning for and mapping to FPGA fabric
17. Laws of Boolean algebra
18. Boolean algebra representation of logic circuit and manipulation
19. Canonical forms
20. K-map method for 2-level logic simplification
21. Multi-level logic circuits
22. Bubble-pushing method for converting from AND/OR to NAND/NOR
23. FSM state transition diagram (STD) representation
24. FSM implementation in circuit based on STD
25. FSM one-hot encoding design method
26. FSMs description in Verilog
27. FSM Moore versus Mealy styles
28. Basics of planar CMOS IC processing
29. IC manufacturing trends and scaling
30. Static switch-level complementary CMOS logic gates
31. Transmission-gate logic circuits
32. Tri-state buffers
33. Edge-triggered Flip-flop implementation and operation
34. Maximum clock frequency calculation from circuit parameters
35. Origin of gate-delay and calculation
36. Delay property of wires and rebuffering
37. Circuit register rebalancing
38. Logic delay combined with wires
39. Driving large capacitive loads