EECS 151/251A Homework 8

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Problem 1: Power Distribution [10pts]

Suppose you are designing an ASIC that draws 10 Watts peak power at 1 Volt V_{dd}. You plan to use a process that has the following resistance values for the metal layers:

M1-M3	1.2 Ω/square
M4-M5	0.77 Ω/square
M6-M7	0.50 Ω/square
M9	0.36 Ω/square

To feed the power grid you plan to use 500 wires that are each 0.1mm long and would like to keep the voltage variation to under 10%. In microns, what total width (across all wires) would you need to use for each of the metal layer choices?

Problem 2: Power Distribution [10pts]

For the ASIC design above, you plan to supply V_{dd} and GND to the chip using solder bump connections, each with 25pH of inductance. 50% of the peak power is dynamic switching power. Assume that the peak current rushes into the chip at the beginning of each clock cycle over 250ps. Again, you would like to keep the voltage variation to within 10%. How many bump connections do you need?

Problem 3: Clock Uncertainty [12pts]

For each of the 7 sources of clock uncertainty listed in the lecture notes, explain how each can lead to clock skew, clock jitter, or both.

Problem 4: Clock Load [8pts]

You are designing an ASIC with a total clock load of 10pF based on a clock grid with minimal resistance. With your 7nm Finfet process, a single fin has an R_{eff} of 12KΩ. How many fins would you need in the final stage of the clock driver to achieve a clock rise time (to 50%) of 10ps?

Problem 5: FIFO Design [20pts]

The FIFO block presented in lecture has the following inputs D_{in}, WE (write enable), RST (reset), CLK, RE (read enable), and the following outputs, FULL, EMPTY, D_{out}. Your job is to design a 8-bit wide FIFO based on a simple dual port memory that is 1K by 8-bits. Assume there are two counters that you can use for the read and write pointers. The counters increment on the rising edge of the clock when their clock enable (CE) signal is true. The counters are 10-bits wide and wrap-around to 0 after they reach their max value. You also can use simple flip-flops as flags to hold the state (FULL/EMPTY) of the FIFO. For simplicity, you may assume that the external producer will never write when full and the consumer will never read when empty.

Design the control logic for the FIFO and draw a block diagram of its implementation using the counters, the memory block, and your control logic.

Problem 6: Memory Blocks [10pts]

You are given a memory block that is 256x16. Show how you would use multiple instances to design a memory that is 1Kx32.

Problem 7: Memory Blocks [8pts]

Write the Verilog code for a synchronous read memory block that is 4Kx32 with two read ports.

Problem 8: Memory Implementation

  (a) [15pts] Consider the design of a (very) small asynchrous-read memory block of 4 words by 4-bits each. You want to implement the memory cells as positive edge-triggered flip-flops. Draw the circuit diagram for your design using the flip-flop cells, multiplexers, and logic gates.

  (b) **251A only**. [15pts] Now consider the redesign of the memory from part a) using latches instead of flip-flops. For this design, as above, the write operation occurs on the positive edge of the clock, but now the output data on a read become available after the failing edge of the clock.

Problem 9: Cache Implementation [12pts]

Consider the design of a 32KB direct mapped cache memory, with a block size of 8-Bytes, and a valid bit for each cache block. This cache will be used in a system with a 32 bit address space. How many total bits of memory would be needed to implement the cache? Sketch the block diagram of the cache implementation.