EECS 151/251A Homework 6

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Due Monday, Mar 11$^{\text{th}}$, 2019

Problem 1: Flip-Flop Malfunction [5 pts]

The positive edge triggered flip-flop presented in lecture could malfunction if the output load capacitance is too high. Explain in detail how this failure could occur. Suggest a modification to the circuit that would fix this problem.

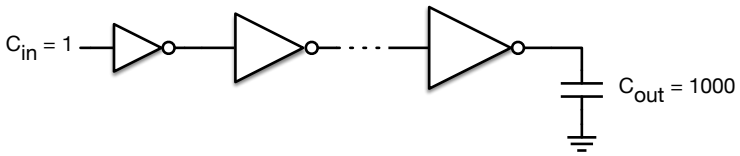
Problem 2: Buffering Long Wires [20 pts]

Assume an inverter (of size 1) is driving another inverter (size 1) through a wire of length L. Because of wire delay you plan to divide the wire into N sections of equal length and insert size 1 inverters as buffers to minimize the total delay. The wire capacitance per unit length is c_w and resistance per unit length is r_w. Assume that the inverter input capacitance $C_g = 10c_w$ and the inverter drive resistance $R_{dr} = 100r_w$. Also assume that the internal capacitance $C_{int} = C_g$.

Derive an expression for N as a function of L that minimizes the delay.

Problem 3: Buffer Chain [5 pts]

Assume that we have the situation shown below with an inverter chain used to drive a large capacitive load (F = 1000) with minimal delay. How many buffers (inverter stages) would be optimal (or near optimal) in this case? What should be the fanout, f, be at each stage?



Problem 4: Gate Propagation Delay Derivation [30 pts]

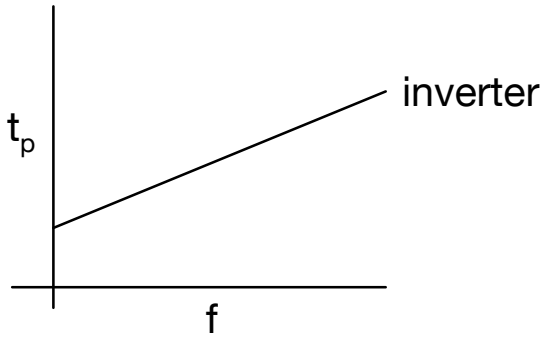
Derive the formulas for gate propagation as a function of fanout, f, for a 2-input NAND gate and a 2-input NOR gate as we did in lecture for the inverter. In both cases, derive the equations based on the input connected to the transistor closest to the output. In the case of the NAND gate assume the other input had been set to 1 (for a long time), and for the NOR, assume the other input had been set to 0. Size the transistors so that the capacitance of each gate input is equivalent to the

input capacitance of the inverter. Also assume that the resistance of the pFET is twice that of the nFET ($Rp = 2Rn$) if the pFET and nFET have the same width. Size the transistors so that the rise time and fall times are equivalent. (Note: For this problem, when 2 transistors are in series, ignore the capacitance at their shared node.)

(a) 2-input NAND equation: t_p =?

(b) 2-input NOR equation: t_p =?

(c) Sketch the curves for the NAND and NOR



(d) **251A only — *Optional* Challenge Question for 151:** Without working it out in detail, sketch the curve you would expect for a 4-input NAND.

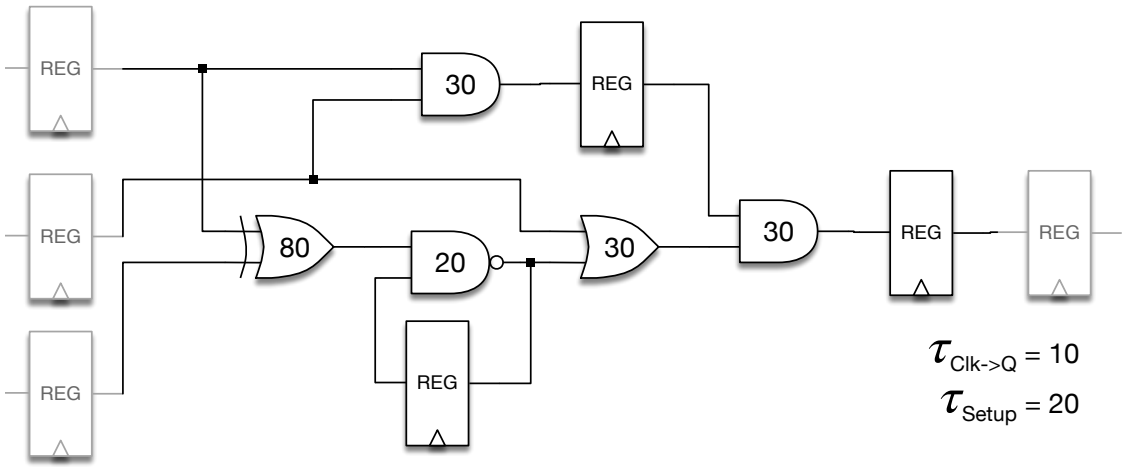
(e) **251A only — *Optional* Challenge Question for 151:** Now assume that for the 2-input NAND we were to consider the other input (the one furthest away from the output). Without working it out in detail, explain how it would effect the result.

Problem 5: Critical Path & Retiming [10 pts]

A circuit for a hypothetical process is shown below. The gate delay (in ps) is written in each gate.

(a) Without modifying the circuit, derive the maximum clock frequency.

(b) Now retime the circuit (without changing the latency between any input and the output) to maximize the clock frequency. Assume that you cannot move the gray registers on the border of the circuit. Draw the new circuit and derive the new maximum clock frequency.


REG
REG
REG
30
REG
80
20
30
30
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REG
$\tau_{Clk->Q} = 10$
$\tau_{Setup} = 20$