EECS 151/251A Homework 5

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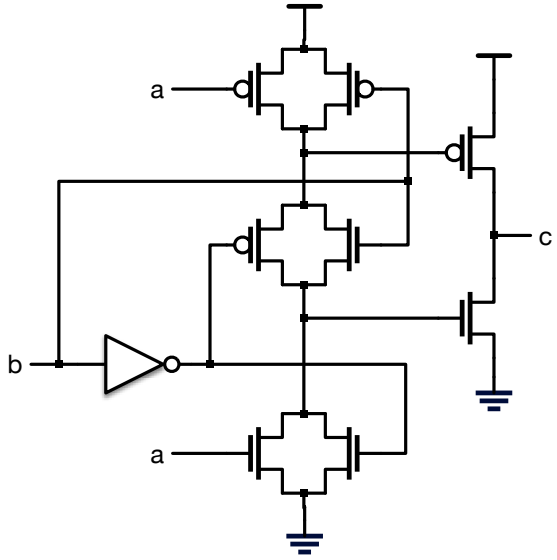
Due Monday, Mar 4th, 2019

Problem 1: Identifying Functions

The circuit shown below implements a common familiar function.

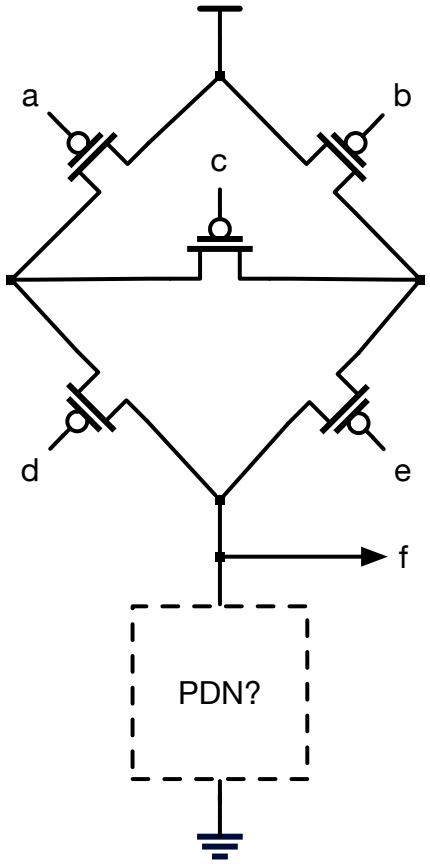


(a) What is the function? Describe the use of a, b, and c.

(b) Why does this implementation provide some advantage over the more common implementation of the same function?

Problem 2: 251A only — *Optional* Challenge Question for 151

The circuit below is an incomplete design of a complementary static CMOS logic gate.



(a) Complete the circuit design by drawing the pull-down network.

(b) What is the Boolean function this gate implements?

Problem 3: Transistor Level Implementation of Logic Gate

Exclusive-nor (XNOR) is defined as the complement of exclusive-or. Draw a complementary static CMOS gate that implements XNOR(a,b) with the minimum number of transistors. You may assume that both inputs a and b are available in uncomplemented and complemented forms.

Problem 4: Transistor Level Implementation of Logic Function

Assuming the inputs are available in uncomplemented and complemented forms, draw a complementary static CMOS gate that implements the majority function of three inputs a, b, and c, using the minimum number of transistors.

Problem 5: Transistor Level Implementation of Logic Function

Assuming that only uncomplemented inputs are available, draw a complementary static CMOS gate that implements $F = (a + b)' + (c + d)'$, using the minimum number of transistors.

Problem 6: Transistor Level Implementation of Logic Function

Assuming that only uncomplemented inputs are available, draw a complementary static CMOS gate that implements $F = a'b'd' + a'b'e' + a'c'f' + a'c'g'$, using the minimum number of transistors.

Problem 7: Pass-Transistor Implementation of Flip-Flop with CE

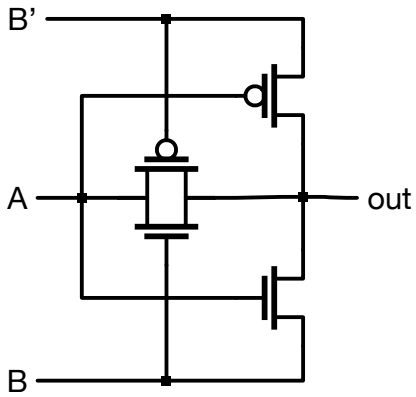
Draw the CMOS positive-edge triggered Flip-flop implementation shown in class (lecture 9) as we did using inverters and transmission gates. Show how you would modify it to include the clock enable (CE) input. You may use additional transistors and gates as needed.

Problem 8: Pass-Transistor Implementation of Flip-Flop with rst

Draw the CMOS positive-edge triggered Flip-flop implementation shown in class (lecture 9) as we did using inverters and transmission gates. Show how you would modify it to include the reset (rst) input. You may use additional transistors and gates as needed.

Problem 9: 251A only — *Optional* Challenge Question for 151

Shown below is a pass-transistor-logic version of a XNOR gate (note this is not a complementary static CMOS gate). Make sure you understand the operation of this gate, then use the concepts in the XNOR gate to design a pass-transistor version of an AND gate implementing AND(A, B).



Problem 10: Transistor Level Implementation of Shifter

Using only transistors, show how you would implement a combinational logic circuit for a variable left-shifter as shown below. X is a 4-bit input, Y is a 4-bit output, and S is a 2-bit control signal that indicates a shift amount of 0, 1, 2, 3 bit positions. Design your circuit to minimize the delay X to Y.