# FPGA Lab - Final Project Checkoff Logistics

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Hi Everyone,
As a reminder, the final project checkoff for the FPGA lab will be occurring next week. The final checkoff is your opportunity to show off all the hard work you have put into the project. I wanted to take a moment to talk about some of the logistics for next week as well as what to expect from the checkoff process.

## 1 Signing-up for a checkoff time:

Checkoffs will be by appointment on Wednesday (5/8) and Thursday (5/9) of RRR week. *One member* of each group should sign up for a time slot by visiting `https://calendar.google.com/calendar/selfsched?sstoken=UUNMVmVKWGU1Rm9jfGRlZmF1bHR8ODQ0YWVhYmNjMjEzZjQ3YzZiOTkyMTYxNjI0ZTVjYmU`. Make sure you are looking at the week of 5/8 & 5/9 in the calendar view and click on an appointment slot that works for you. If none of the available slots work for your group, please let me know.

## 2 What to expect during checkoff:

You will be asked to run several demos of your processor implementation on the FPGA *including*:

- Running the mmul program (this will be used as the basis for evaluating CPU optimizations along with the achieved clock rate)
- Running the user_io_test program
  - Demonstrating LED set
  - Demonstrating button read
  - Demonstrating switch read
- Running the graphics program
  - Filling the screen with a solid color
  - Drawing several lines using swline
  - Setting a few pixels
  - Drawing a line using your line drawing accelerator (using a modified version of the graphics program which can leverage your accelerator.
- Running a program provided by you which demonstrates an extra credit feature *(only if you did extra credit).*

You will be asked about the details from Vivado reports *including*:

- Resource Usage (especially number of LUTs)
- Achieved clock rate
- Timing closure (yes/no, by how much)

You will be asked some questions about your design.

- For example: how does your processor deal with load hazards?

You will also be asked about your experience implementing the project *including*:

- What was your strategy for working in a group (if applicable)?
- How long did you expect different parts of the project to take? How well did that line up with reality?
- What parts of the project were the most/least time consuming?

## 3 Advice for priorities leading up to checkoff:

The bulk of the project grade comes from demonstrating a functional processor which is capable of executing a program. Your first priority should be getting a working processor implementation which can execute the bios, mmul, and echo programs. Once you have that working reliably, you can move on to integrating the I/O and optimizing the design.

*Note that demonstrating a functioning processor with no I/O (except UART) and a high CPI is much better than showing a non-functional CPU with everything theoretically implemented.*

If you feel that you are stuck getting your processor implementation working, please let me know so I can try to help you get moving again.

## 4 Tips for a successful checkoff:

- As you modify your processor leading up to checkoff, it is easy to make changes that break functionality that was previously working. This can lead to your processor failing to demonstrate basic functionality during checkoff, which represents the bulk of the project grade. **To avoid this, make sure you have backup copies of your design and .bit files that you have thoroughly tested and know work.**
- Make sure you have the Vivado implementation reports generated and ready to show.
- Refresh your memory about your processor design and implementation beforehand so that you are ready to answer questions.