EECS 151/251A Final Exam Information

Exam Date: May 17th, 2019

The exam will take place Friday May 17, 7–10PM in Hearst Gym 251. The exam comprises a set of questions with 1 point per expected minute of completion with a total of approximately 90 points. 251A students will be asked to complete extra questions. All students are allowed one 2-sided 8.5×11 inch sheet of notes. No calculators, phones, or other electronic devices will be allowed. Slide-rules will be permitted.

Topics:

The final exam will be comprehensive and test all topics covered this semester. However, emphasis will be placed on topics covered after the midterm exam—those listed below.

1. Sources of Power and Energy consumption in Digital ICs
2. Principles Behind Six Low-power Design Techniques
3. How to Improve Energy Efficiency through Parallelism and Pipelining
4. How to Design a RISC-V Single-Cycle Processor from the ISA
5. Processor Pipelining Hazards and Mechanisms
6. Principle behind and motivations for hardware acceleration
7. Line Drawing Accelerator Design Details
8. Memory Block Internal Architecture
9. SRAM Cell and Read/Write Operation
10. Memory Block Periphery Circuits
11. Memory Decoder Design
12. DRAM Cell and Read/Write Operation
13. Dual-port Memory Architecture
14. Effect of Clock Uncertainties on Maximum Clock Frequency
15. Source of Clock Uncertainties
16. Principle of Good Clock Distribution
17. IR and dI/dt effects in Power distribution

18. Cascading Memory blocks for More Width, Depth, and Ports
19. FIFO Implementation
20. Memory Block Specification in Verilog
21. Serialization versus Parallelization in Iterative Computations
22. Principles of Pipelining and Restrictions of Loops
23. C-Slow Technique for Pipelining Loops
24. Carry Select Adder Design
25. Carry Lookahead and Parallel Prefix Adders
26. Bit-Serial Addition
27. Array Multiplier Design
28. Carry Save Addition
29. Signed Multiplication
30. Booth Encoding
31. Bit-Serial Multiplication
32. CSD Multiplier Design
33. Log and Barrel Shifters Design and Analysis
34. Use of Counters in Controller Design
35. Binary Counter Design and Optimization
36. Ring Counter Design
37. LFSR Implementation
38. List Processor Design and Optimizations
39. Modulo Scheduling
40. Types and Sources of Faults in ICs
41. Hamming Codes