

EECS151/251A Discussion 7

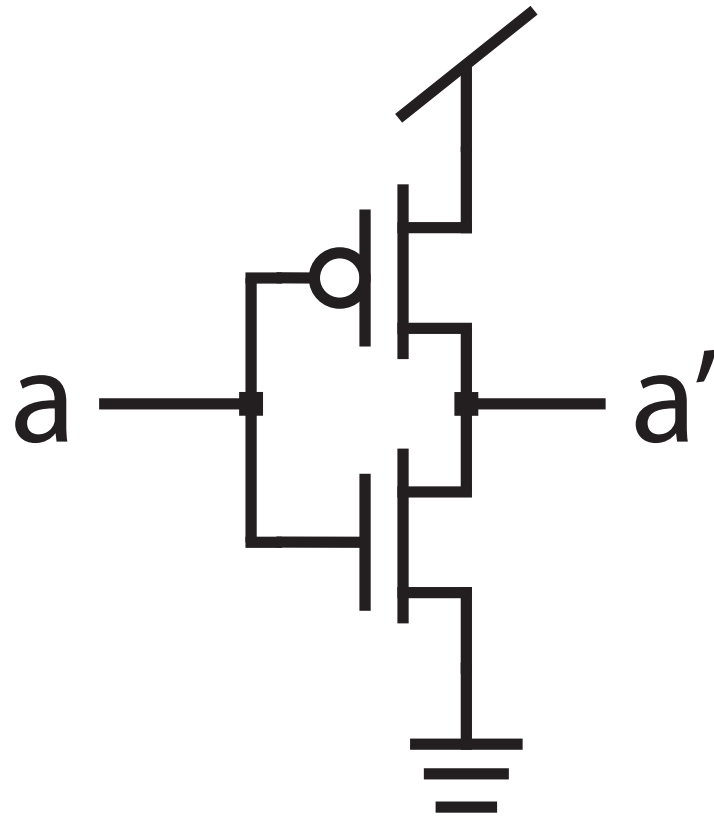
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Mar. 8, 2019

Plan for Today

- Deriving Inverter Characteristics
- Practice Problem
- Your Questions

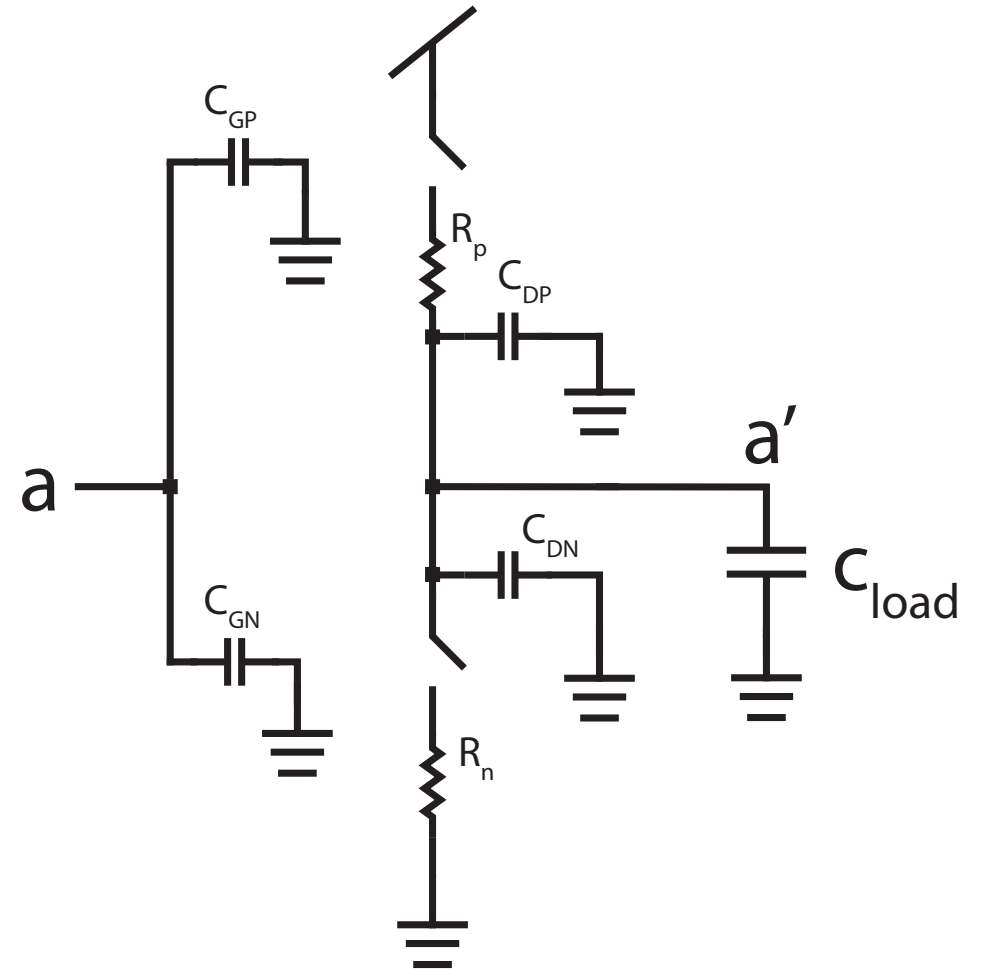
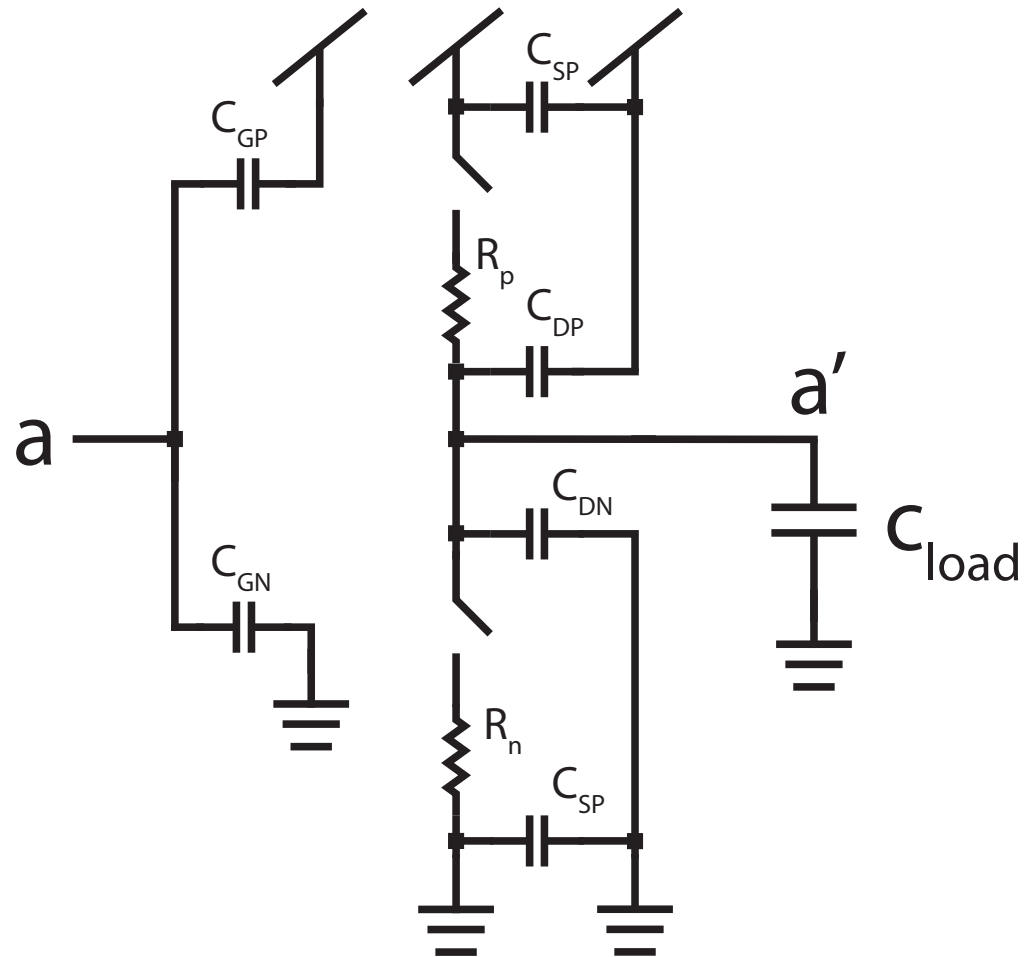
Inverter Characteristics



- For this problem we will assume
 - $R_P = 2R_N$ for equal width transistors
 - Let R_{N0} be the resistance of a unit size N-FET
 - $C_{GP} = C_{GN} = C_G$ for equal width capacitors
 - Let C_{G0} be the gate capacitance of a unit size FET
 - Scaling transistor width by a factor W scales the following parameters
 - $R = \frac{R_{orig}}{W}$
 - $C = WC_{orig}$
 - We will size the width of the N-FET by W and the width of the P-FET by $2W$
- We will characterize the following aspects of the inverter
 - Internal Capacitance
 - Input Capacitance
 - Gate delay as a function of fanout

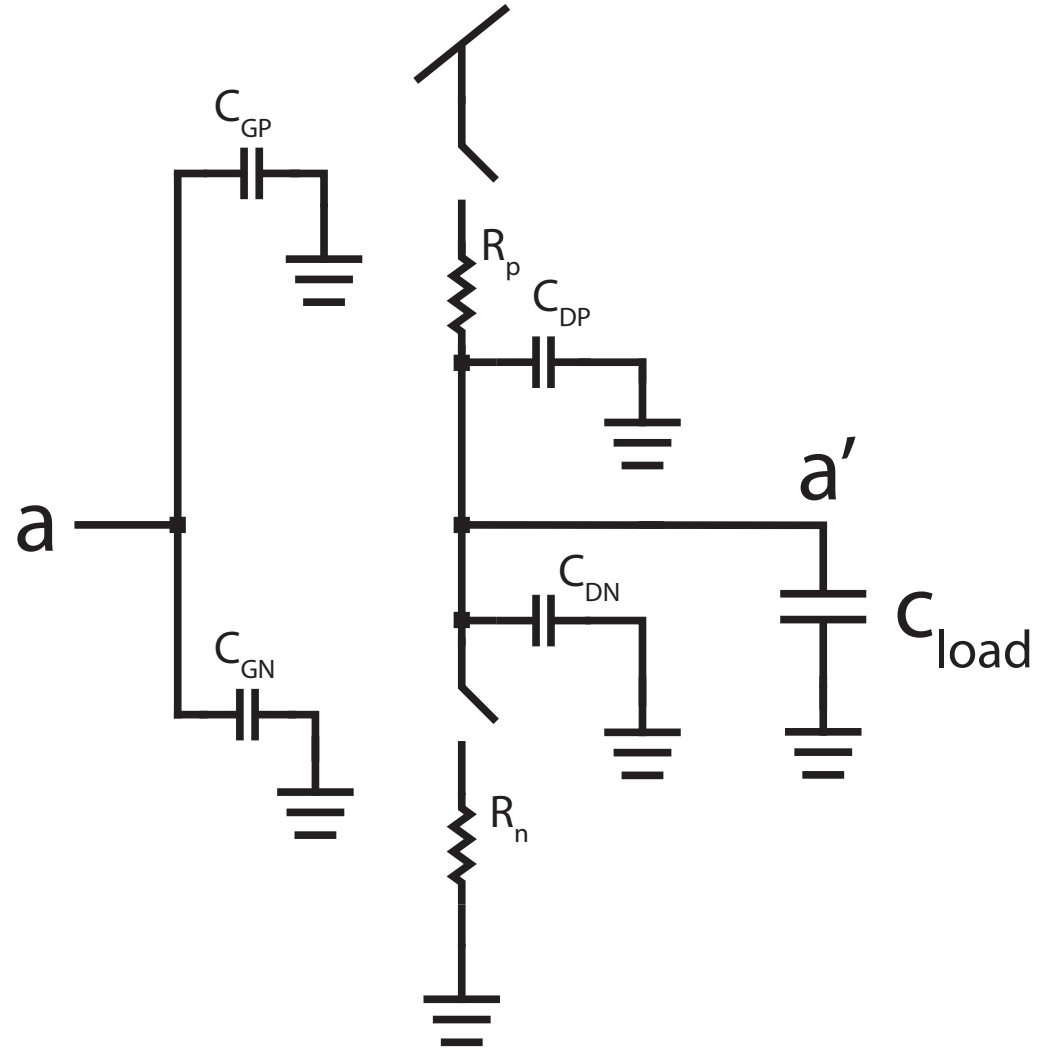
Inverter Parasitics

- The source capacitances are shorted to the voltage ranges and can be ignored
- An equivalent model can be made by tying all capacitors connected to static voltage rails to ground (see Weste & Harris pg 144)



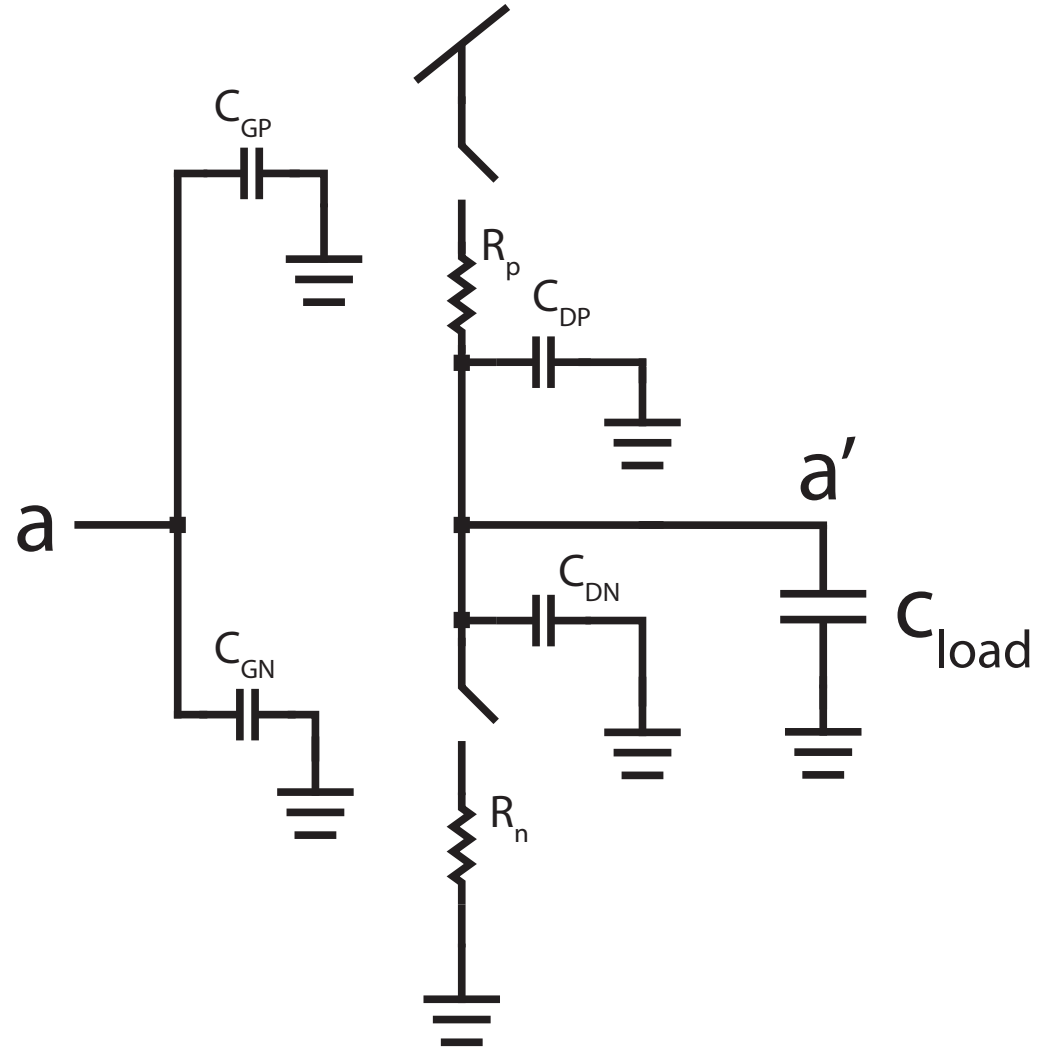
Input Capacitance

- Width N-FET = W
- $C_{GN} = WC_{G0}$
- Width P-FET = $2W$
- $C_{GP} = 2WC_{G0}$
- $C_{in} = C_{GP} + C_{GN} = 3WC_{G0}$
(Parallel Capacitance)



Internal Capacitance

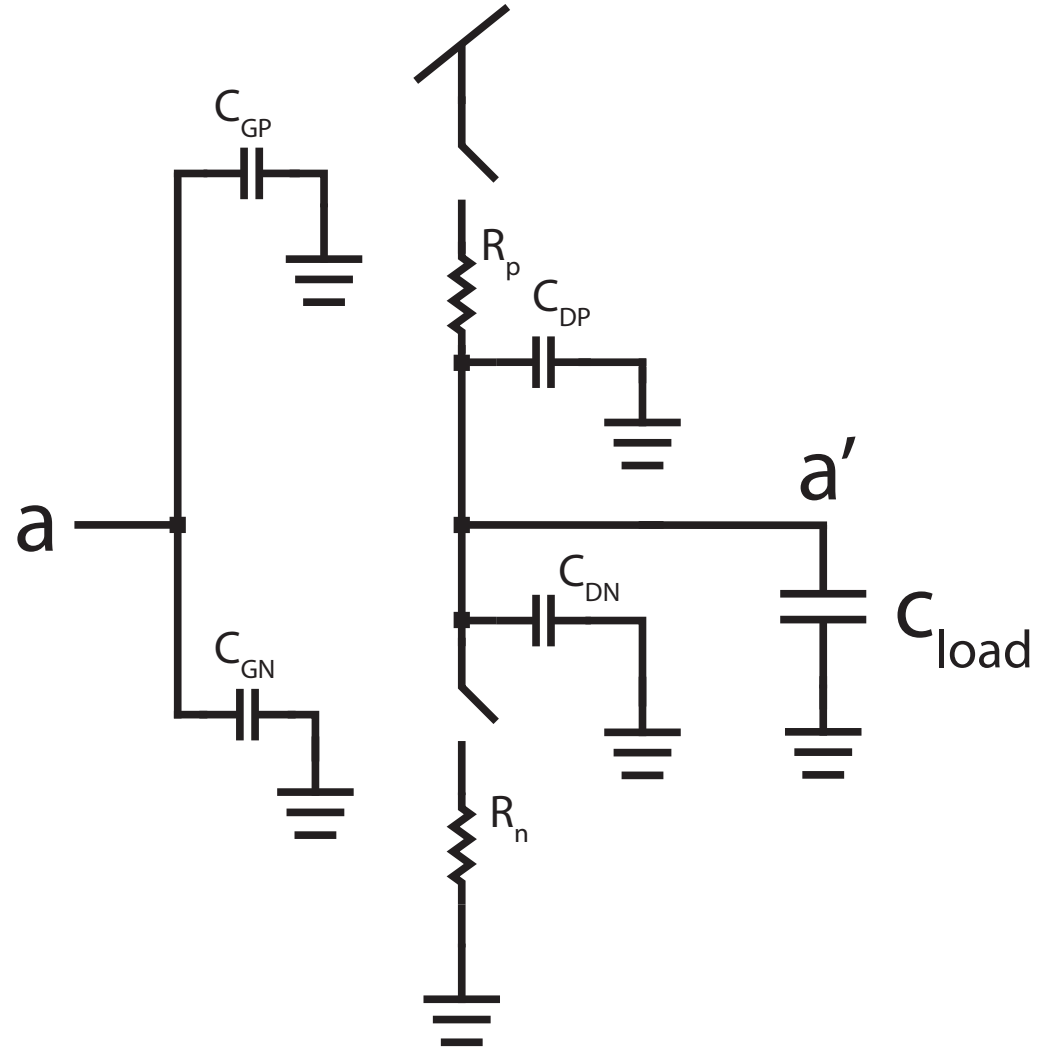
- $C_D = \gamma C_G$
- Width N-FET = W
- $C_{DN} = W\gamma C_{G0}$
- Width P-FET = $2W$
- $C_{DP} = 2W\gamma C_{G0}$
- $C_{int} = C_{DP} + C_{DN} = 3W\gamma C_{G0}$
(Parallel Capacitance)



Output Capacitance

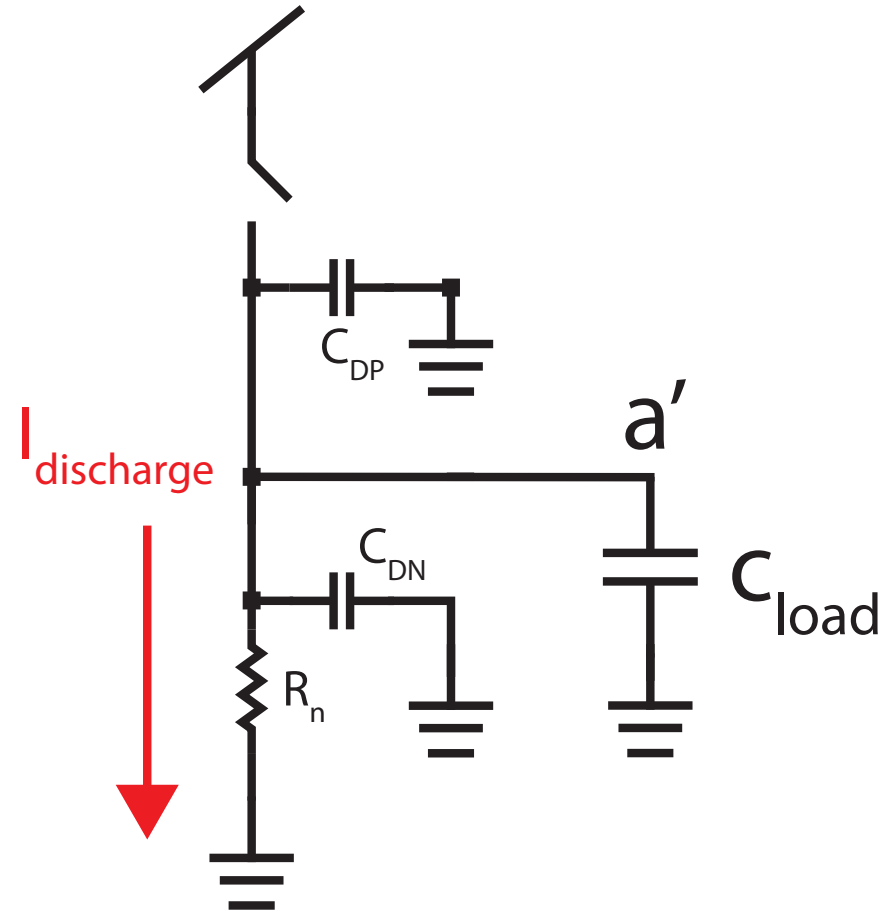
- $C_{out} = C_{int} + C_{load} = 3W\gamma C_{G0} + C_{load}$

(Parallel Capacitance)



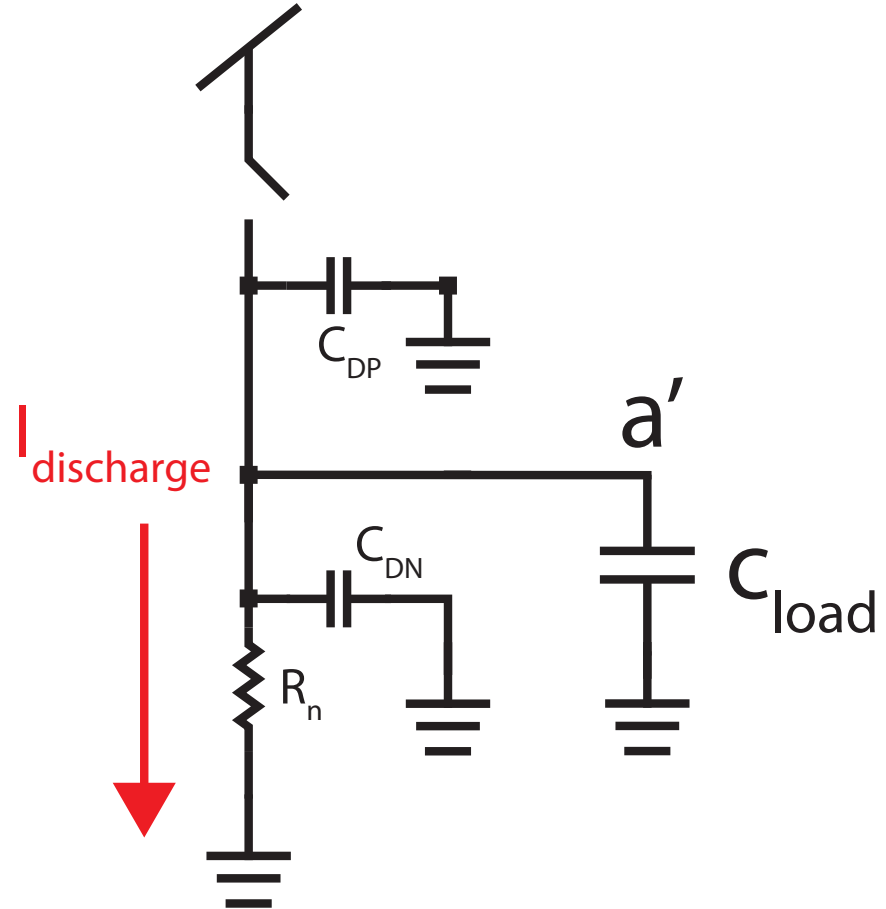
Discharge Time

- How long does it take to discharge the output to $V_{DD}/2$?
- This looks like an RC circuit!
- $R_N = R_{N0}/W$
- $C_{out} = 3W\gamma C_{G0} + C_{load}$
- $V = V_{DD}e^{-t/(R_N C_{out})}$
- Solve for t when $V = 0.5V_{DD}$



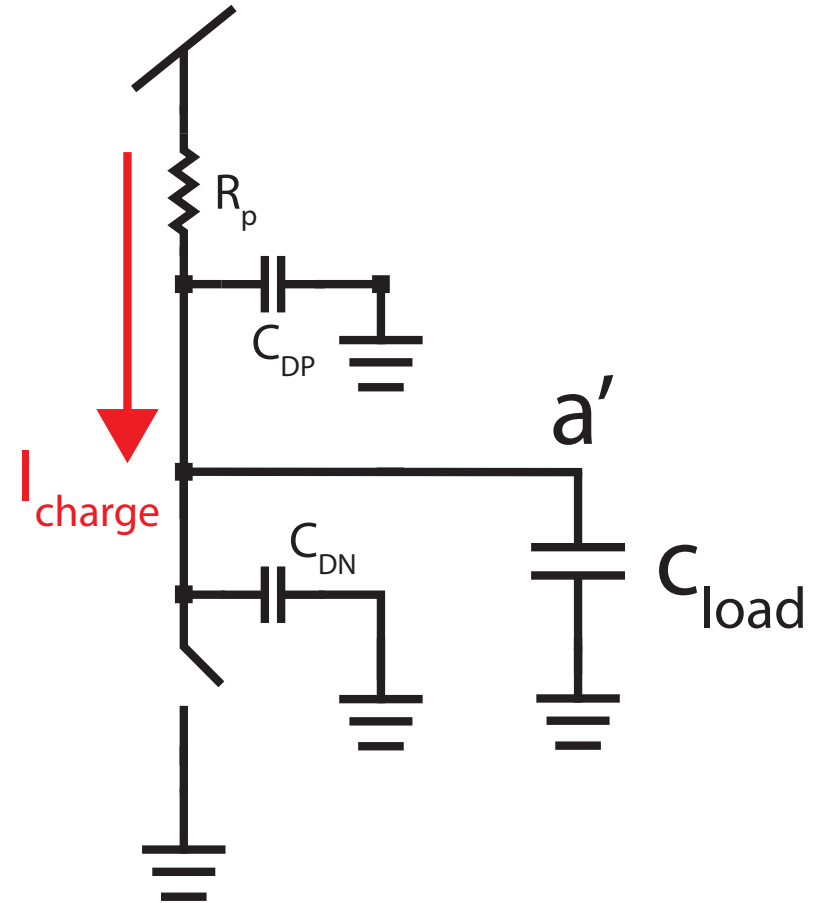
Discharge Time

- Solve for t when $V = 0.5V_{DD}$
 - $0.5V_{DD} = V_{DD}e^{-t/(R_N C_{out})}$
 - $0.5 = e^{-t/(R_N C_{out})}$
 - $\ln(0.5) = -t/(R_N C_{out})$
 - $t = -\ln(0.5)(R_N C_{out})$
 - $t = -\ln(0.5)(R_{N0}/W)(3W\gamma C_{G0} + C_{load})$
 - $t = -\ln(0.5)(3R_{N0}\gamma C_{G0}) \left(1 + \frac{C_{load}}{3W\gamma C_{G0}}\right)$
 - Recall that $C_{in} = 3W C_{G0}$
 - $t = -\ln(0.5)(3R_{N0}\gamma C_{G0}) \left(1 + \frac{C_{load}}{\gamma C_{in}}\right)$
 - Recall fanout: $f = \frac{C_{load}}{C_{in}}$
 - $t = -\ln(0.5)(3R_{N0}\gamma C_{G0}) \left(1 + \frac{f}{\gamma}\right)$
 - $t \approx 0.69(3R_{N0}\gamma C_{G0}) \left(1 + \frac{f}{\gamma}\right)$



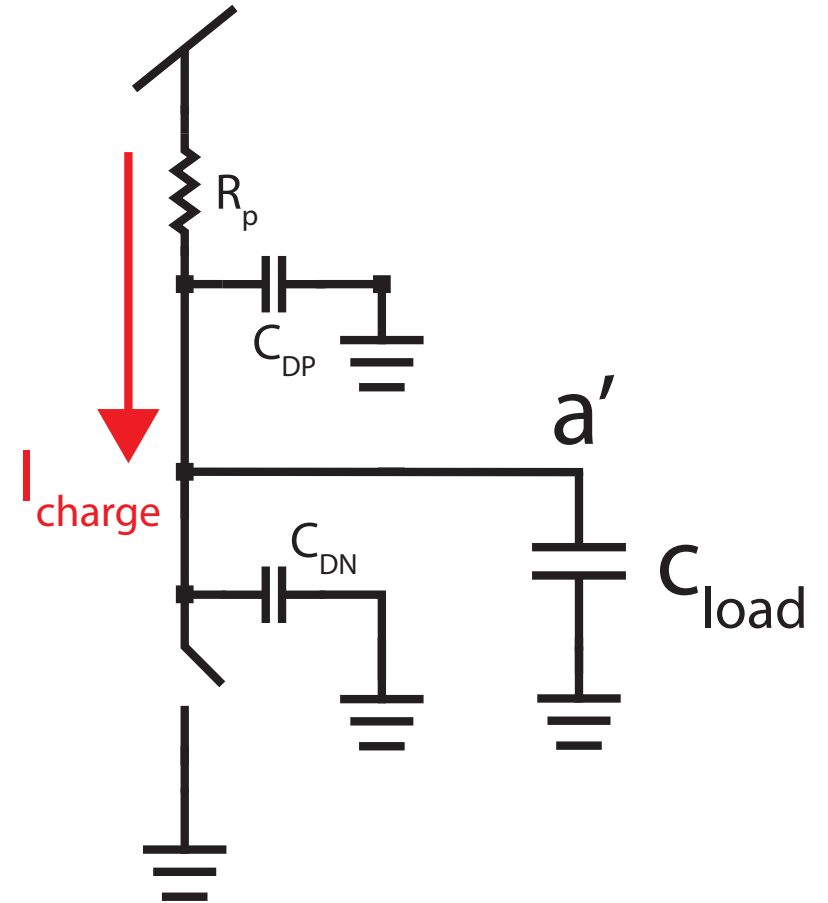
Charge Time

- Similar to discharge time
- How long does it take to charge the output to $V_{DD}/2$?
- This looks like another RC circuit!
- $R_{P0} = 2R_{N0}$
- $R_P = \frac{R_{P0}}{2W} = \frac{2R_{N0}}{2W} = \frac{R_{N0}}{W}$
- $C_{out} = 3W\gamma C_{G0} + C_{load}$ (same as before)
- $V = V_{DD}(1 - e^{-t/(R_P C_{out})})$
- Solve for t when $V = 0.5V_{DD}$



Charge Time

- Solve for t when $V = 0.5V_{DD}$
 - $0.5V_{DD} = V_{DD}(1 - e^{-t/(R_P C_{out})})$
 - $0.5 = 1 - e^{-t/(R_P C_{out})}$
 - $0.5 = e^{-t/(R_P C_{out})}$
 - $\ln(0.5) = -t/(R_P C_{out})$
 - $t = -\ln(0.5)(R_P C_{out})$
 - $t = -\ln(0.5) (R_{N0}/W)(3W\gamma C_{G0} + C_{load})$
 - Note that this is the same expression we had when calculating discharge time
 - $t = -\ln(0.5)(3R_{N0}\gamma C_{G0}) \left(1 + \frac{f}{\gamma}\right)$
 - $t \approx 0.69(3R_{N0}\gamma C_{G0}) \left(1 + \frac{f}{\gamma}\right)$



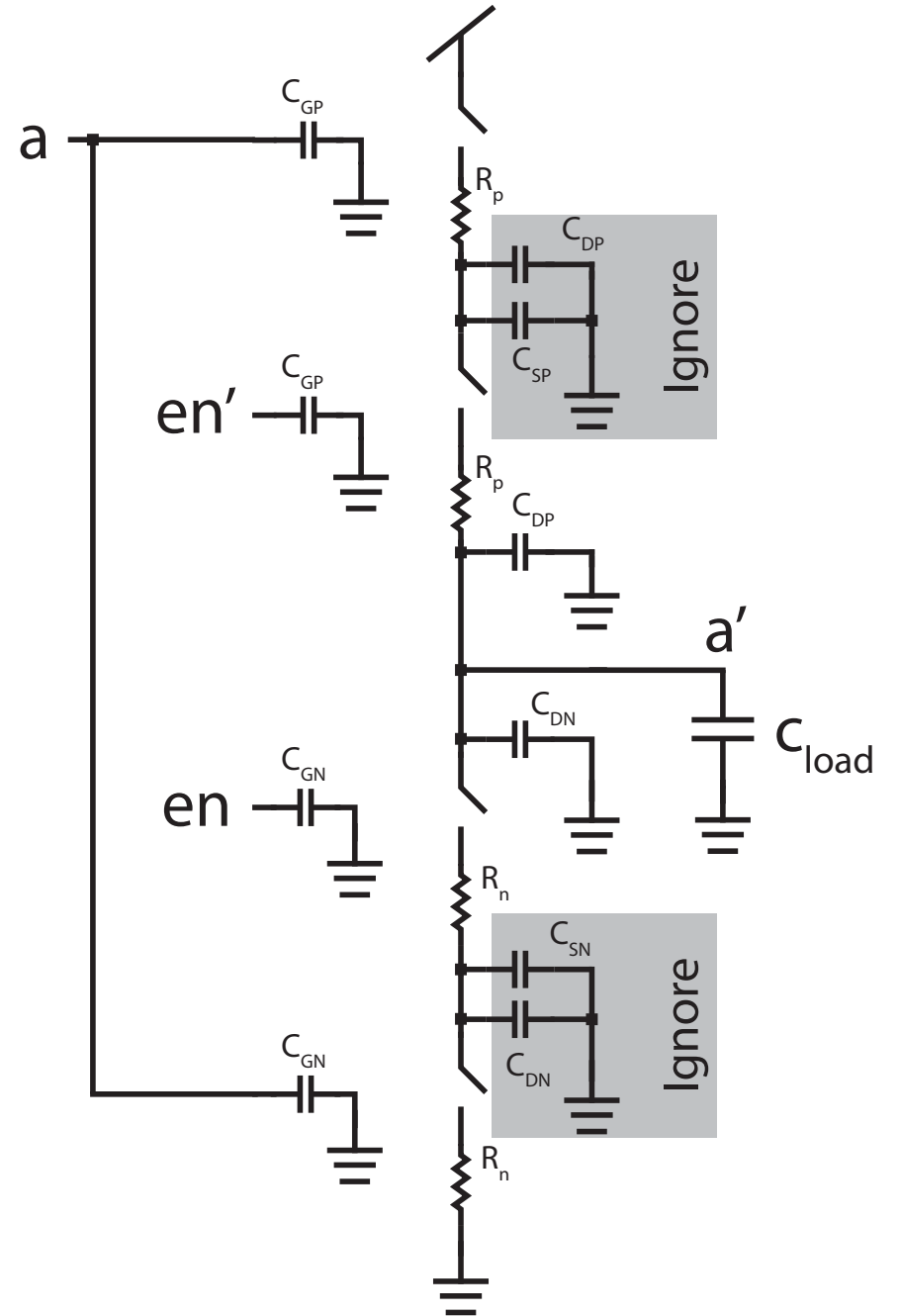
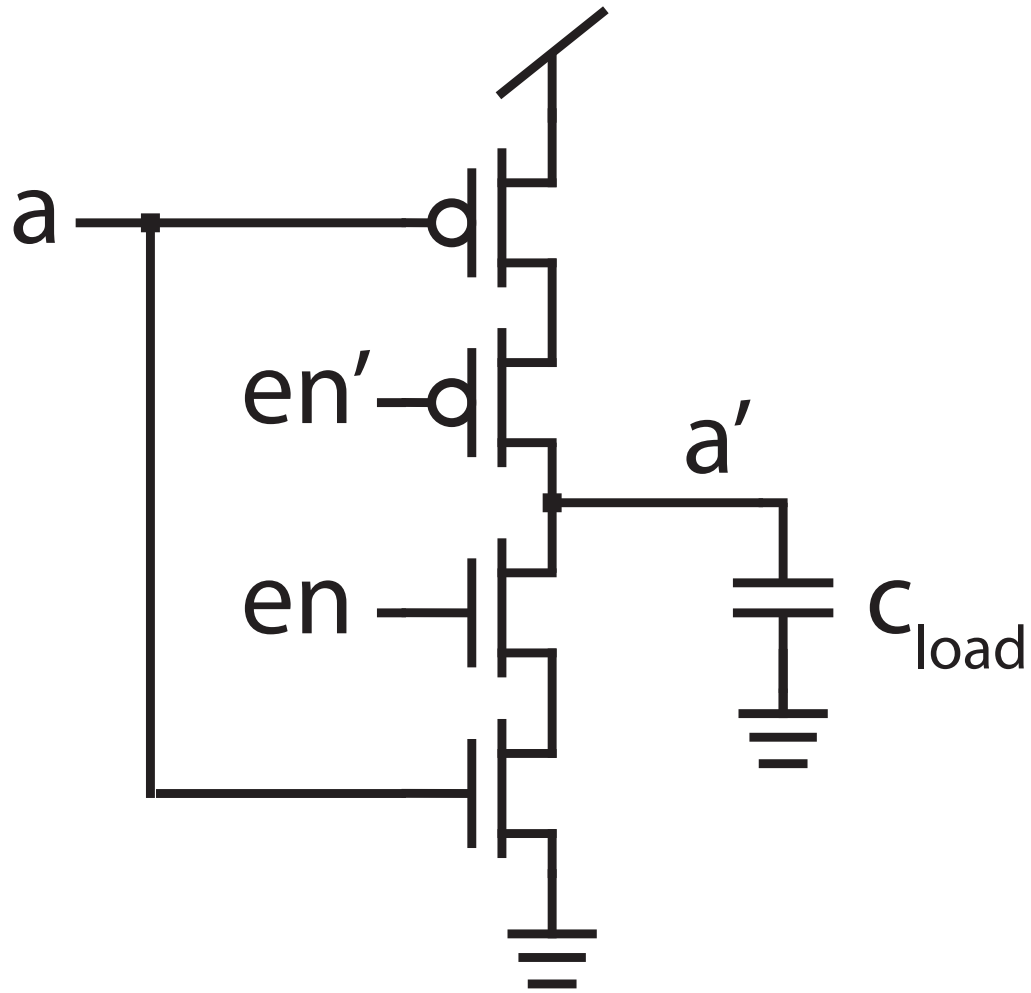
Notes on the Inverter

- The sizing of the P-MOS to be 2x the width of the N-MOS was not an accident!
- It caused the charge time and discharge times to be balanced
- Generally, we try to design gates that exhibit balanced charge and discharge time

More Complex Gates – Tristate Inverter

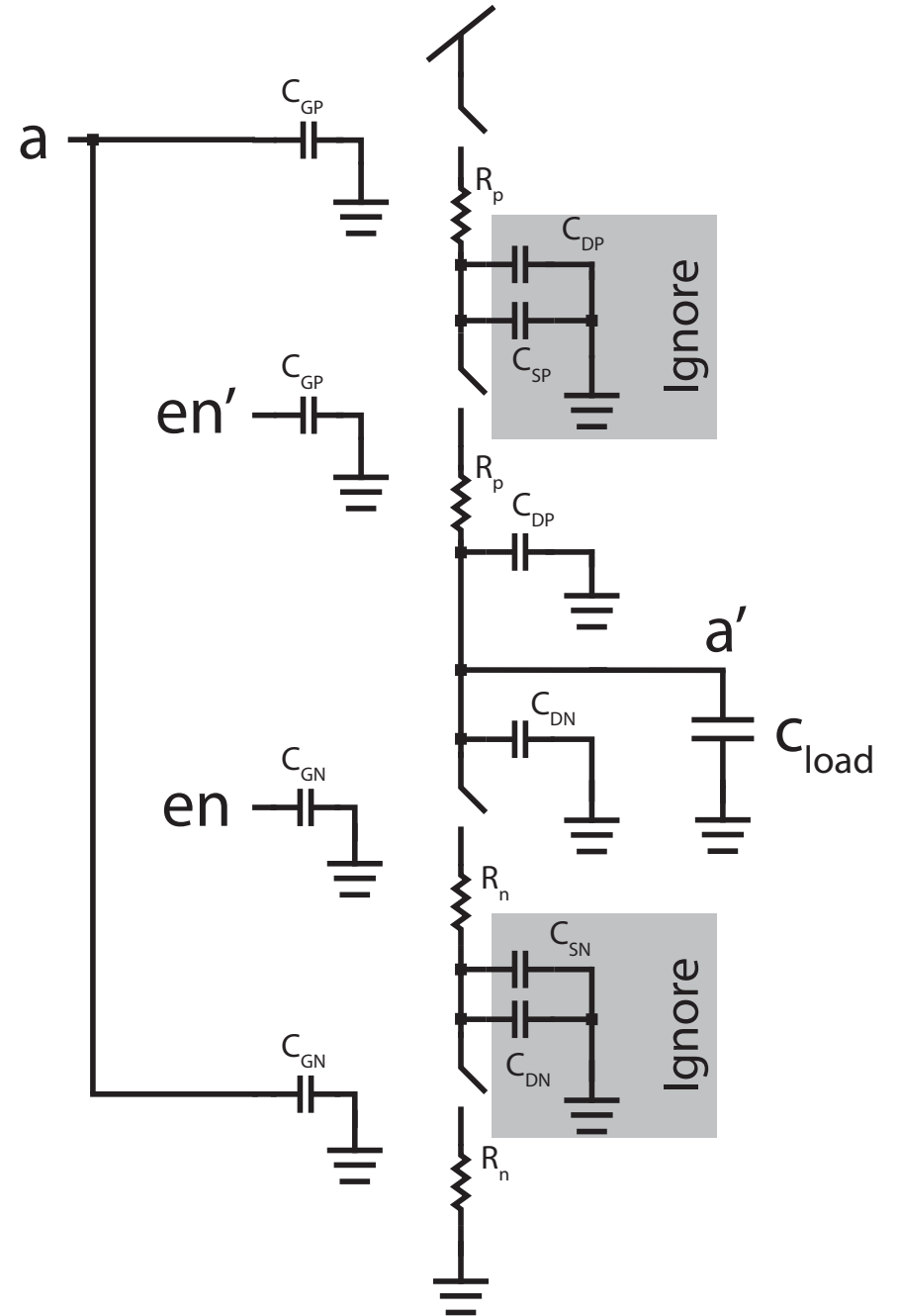
- Characterize the delays for a tristate inverter from its enable input
 - Assume both complemented and uncomplemented inputs are available
 - Assume the output has been discharged by another circuit when calculating the charge time
 - Assume the output has been charged to V_{DD} when calculating the discharge time
- You can ignore the capacitance at intermediate nodes between transistors in series for this problem ... more on this later

Tristate Inverter Model



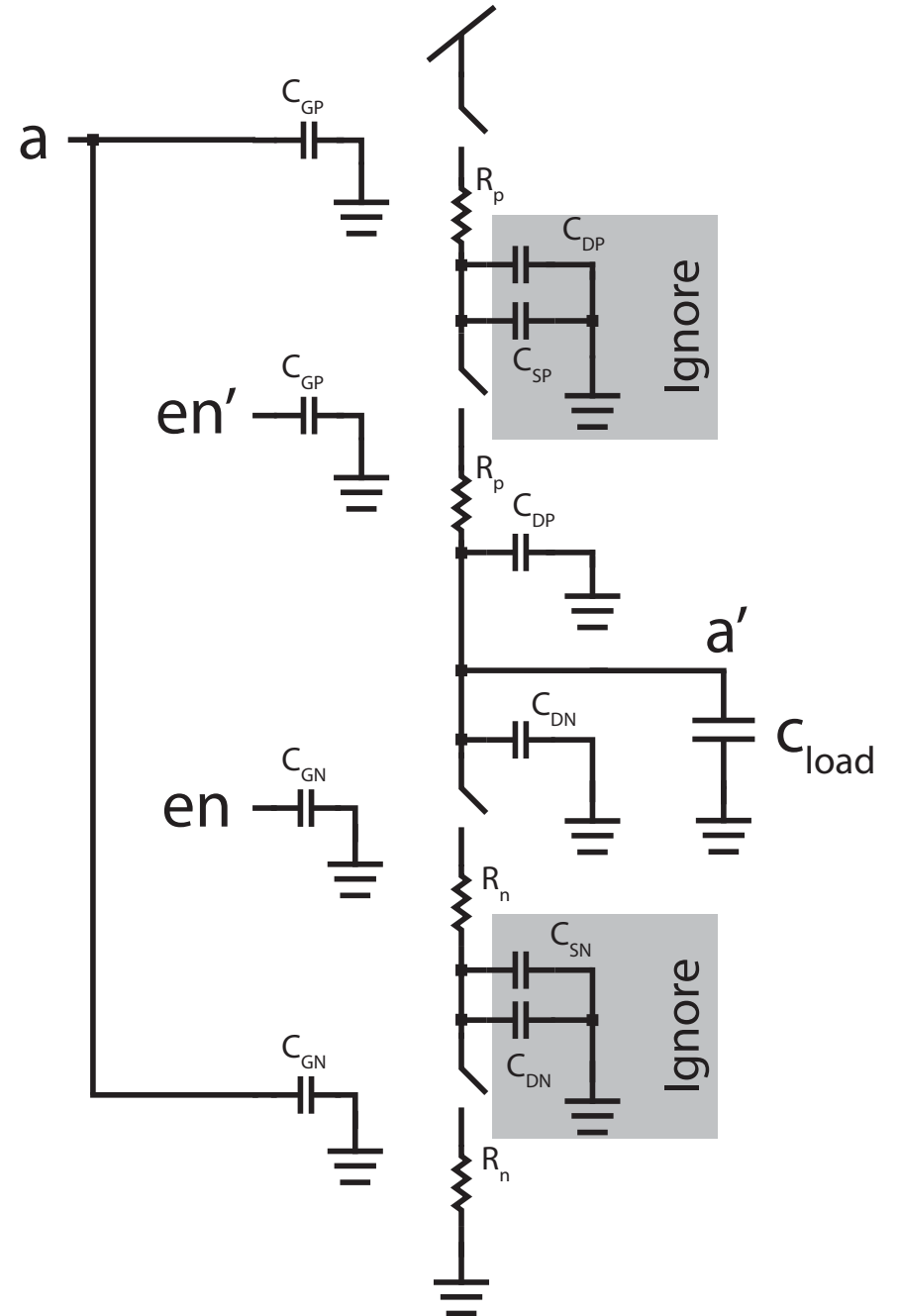
Calculating Resistance

- Width N-FET = W
- $R_N = \frac{R_{N0}}{W}$
- Width P-FET = $2W$
- $R_{P0} = 2R_{N0}$
- $R_P = \frac{R_{P0}}{2W} = \frac{2R_{N0}}{2W} = \frac{R_{N0}}{W}$



Calculating Capacitance

- $C_D = \gamma C_G$
- Width N-FET = W
- $C_{DN} = W\gamma C_{G0}$
- Width P-FET = $2W$
- $C_{DP} = 2W\gamma C_{G0}$
- $C_{int} = C_{DP} + C_{DN} = 3W\gamma C_{G0}$
- $C_{out} = C_{int} + C_{load} = 3W\gamma C_{G0} + C_{load}$



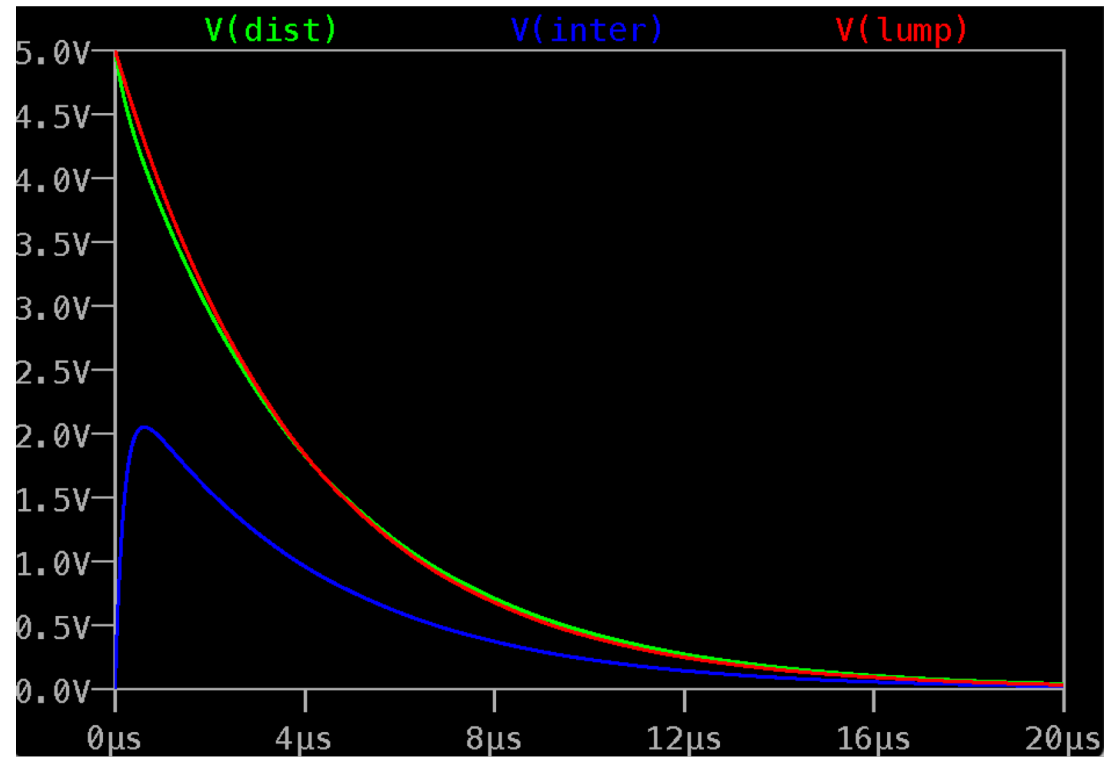
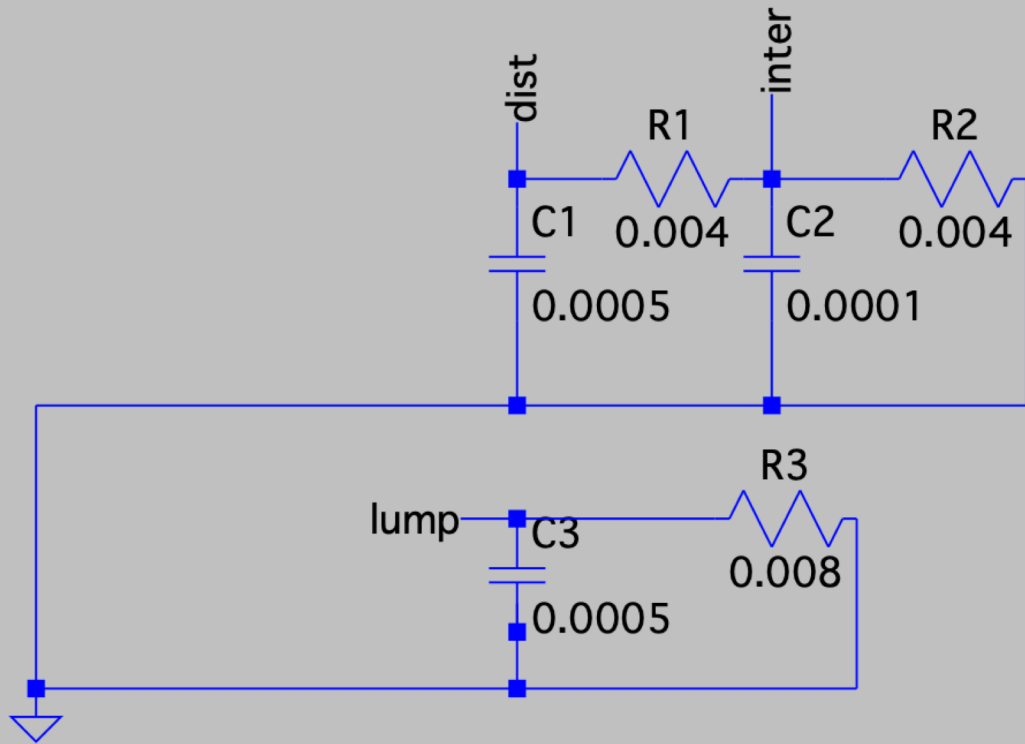
Ignoring the Intermediate Node Capacitance

- When we have transistors in series, there exists some parasitic capacitance at the intermediate node they share
- This capacitance stops us from using simple first order RC charge/discharge equations because we now need to account for charge that is stored in the intermediate node capacitance
- For small intermediate node capacitance values, ignoring this second order effect will not change the calculated propagation delay by too much*
- For a more accurate first order approximation that does not completely ignore the intermediate node capacitance, see Weste & Harris pg. 150.

Quick aside to (LT)SPICE!

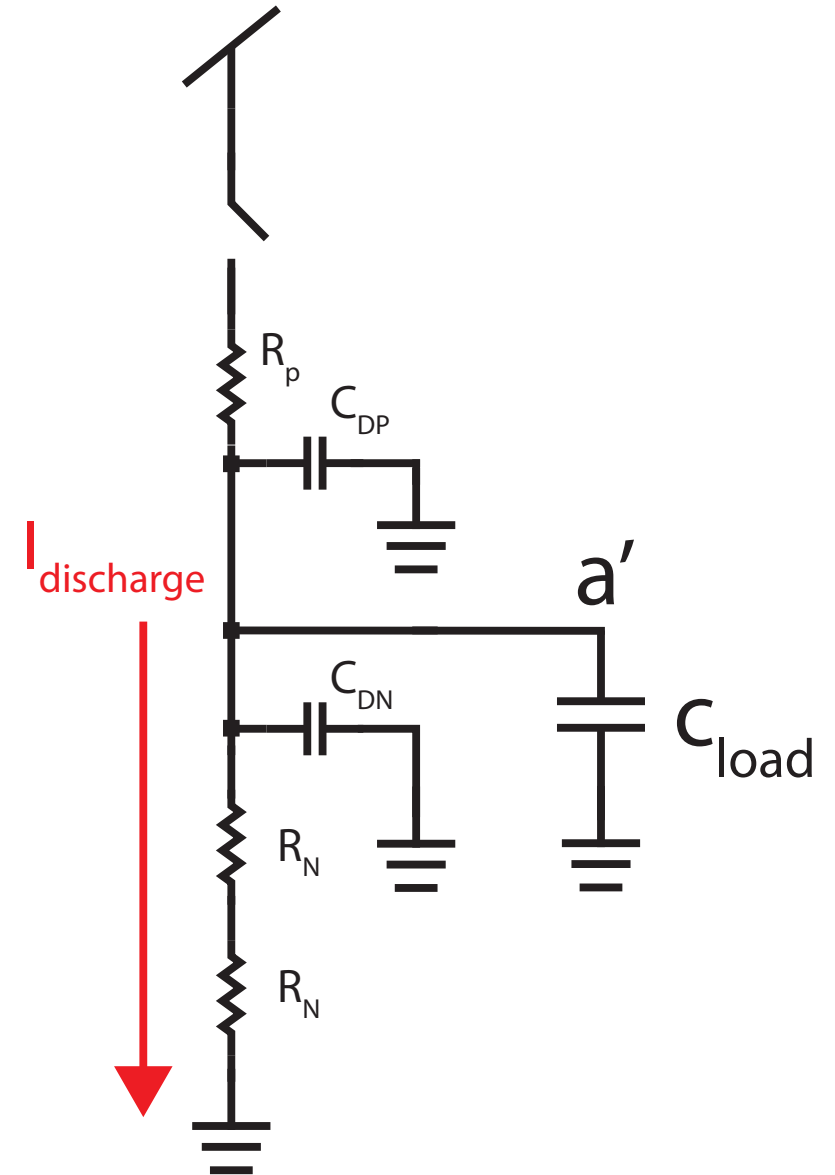
```
.TRAN 0.0000001 0.00002
```

```
.IC V(inter)=0, V(dist)=5, V(lump)=5
```



Discharge Time

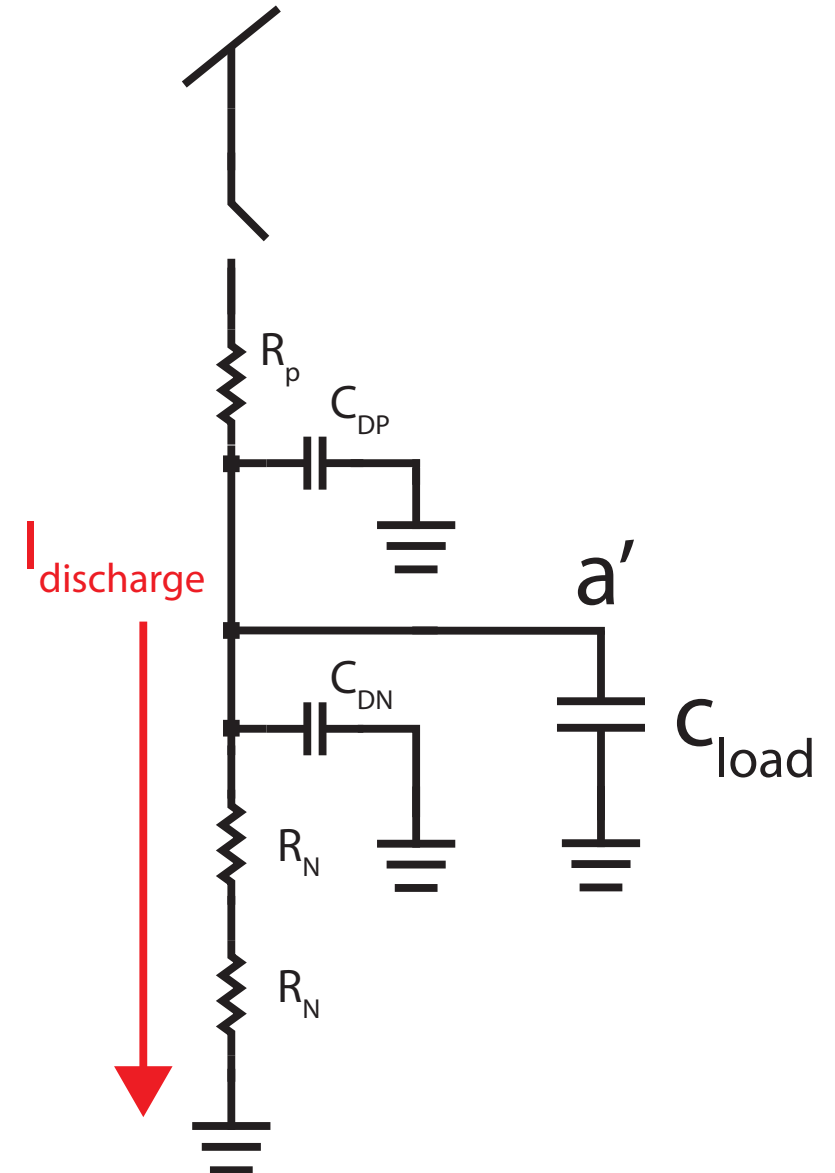
- How long does it take to discharge the output to $V_{DD}/2$?
- This looks like another RC circuit!
- Except, this time, we have series resistance we need to consider
- $R = 2R_N = 2R_{N0}/W$
- $C_{out} = 3W\gamma C_{G0} + C_{load}$
- $V = V_{DD}e^{-t/(RC_{out})} = V_{DD}e^{-t/(2R_N C_{out})}$
- Solve for t when $V = 0.5V_{DD}$



Discharge Time

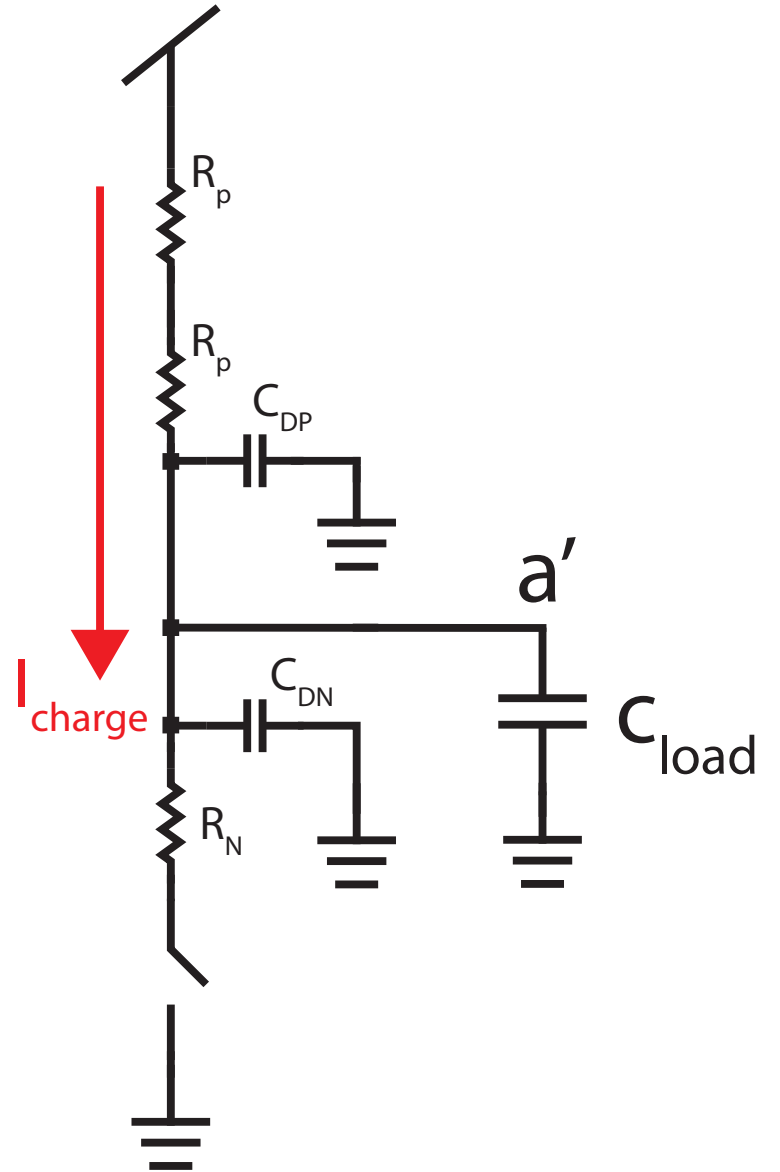
- Solve for t when $V = 0.5V_{DD}$
 - $0.5V_{DD} = V_{DD}e^{-t/(2R_N C_{out})}$
 - $0.5 = e^{-t/(2R_N C_{out})}$
 - $\ln(0.5) = -t/(2R_N C_{out})$
 - $t = -\ln(0.5)(2R_N C_{out})$
 - $t = -\ln(0.5)(2R_{N0}/W)(3W\gamma C_{G0} + C_{load})$
 - $t = -\ln(0.5)(6R_{N0}\gamma C_{G0}) \left(1 + \frac{C_{load}}{3W\gamma C_{G0}}\right)$

Compared to the inverter, this term is 2x larger



Charge Time

- How long does it take to charge the output to $V_{DD}/2$?
- This looks like another RC circuit!
- Except, this time, we have series resistance we need to consider
- $R = 2R_P = 2R_{N0}/W$
- $C_{out} = 3W\gamma C_{G0} + C_{load}$
- $V = V_{DD}(1 - e^{-t/(2R_P C_{out})})$
- Solve for t when $V = 0.5V_{DD}$



Charge Time

- Solve for t when $V = 0.5V_{DD}$
 - $0.5V_{DD} = V_{DD}(1 - e^{-t/(2R_P C_{out})})$
 - $0.5 = 1 - e^{-t/(2R_P C_{out})}$
 - $0.5 = e^{-t/(2R_P C_{out})}$
 - $\ln(0.5) = -t/(2R_P C_{out})$
 - $t = -\ln(0.5)(2R_P C_{out})$
 - $t = -\ln(0.5) (2R_{N0}/W)(3W\gamma C_{G0} + C_{load})$
 - Note that this is the same expression we had when calculating discharge time
 - $t = -\ln(0.5)(6R_{N0}\gamma C_{G0}) \left(1 + \frac{C_{load}}{3W\gamma C_{G0}}\right)$

↑
Compared to the inverter, this term is 2x larger

