# EECS 151/251A Discussion 9

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## Problem 1: Embedded Memory Technologies

You have been tasked with creating a CPU for a smart speaker by popular gadget maker Orchard. The product team has determined that the processor requires a 2 MiB (1MiB = 1*1024*1024 bytes) cache to meet the needs of the software application controlling the speaker. It was determined that cache lines should be 32 32-bit words wide. You are currently looking at different techniques to implement the cache.

The silicon foundry includes 6T SRAM cells and 3T DRAM cells in the design kit for the CMOS logic process you are planning to use to implement your processor.

- You want to have an equal number of rows and columns in the memory. How many rows and columns do you need?
- What is the approximate size difference between a SRAM version of the memory and a DRAM version of the memory (assume all transistors are the same size and ignore the periphery logic).
- What are some of the principle disadvantages of the DRAM cell compared to the SRAM cell?
- Why do you suspect the silicon foundry did not provide a 1T DRAM cell for this CMOS logic process?

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