EECS 151/251A Discussion 7

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Problem 1: Characterizing a Gate

In this problem, we will characterize several aspects of a tristate inverter. We will only be characterizing parameters related to the input connected to the transistors closest to the output (the enable input). When calculating discharge time, we will assume the other input a has been set to 1 for a long time and that the output had been driven to V_{DD} by some outside circuit (not shown). When calculating charge time, we will assume a has been set to 0 for a long time and that the output had been driven to ground by some outside circuit (not shown).

For this problem, we will assume both the complemented and uncomplemented versions of en are available and that they change in unison.

We will also assume that, for transistors of equivalent width, $R_p = 2R_n$.

In this problem, the PMOS has a width $2W$ the NMOS has a width of W. We will assume a unit sized (width 1) NMOS has a resistance R_{N0} and the gate capatance C_{G0} This tristate inverter is also connected to a capacitive load of C_{out}.

Note that in this problem, you can make the simplifying assumption that the capacitance at the common node between two series transistors can be ignored.

For this tristate inverter gate, answer the following questions:

(a) What is the effective resistance of the PMOS and the NMOS?

(b) What is the internal capacitance at the output node? What is the total capacitance at the output node?

(c) How much time is required to charge the output to $0.5V_{DD}$ when en switches from 0 to 1, $a = 0$, and the output caries an initial charge of 0?

(d) How much time is required to discharge the output to $0.5V_{DD}$ when en switches from 0 to 1, $a = 1$, output caries an initial charge of V_{DD}?