## EE 42

## Homework \#3 Solutions

## Problem 1:

$\mathrm{V}_{\text {IN,UP }}(\mathrm{t})=5-5 \mathrm{e}^{-2000 \mathrm{t}} \mathrm{V} \quad$ This input is going up from 0 V to 5 V . So will the output.
The output first hits 5 V at the very end of the linear region.
$\mathrm{V}_{\text {OUT }}(\mathrm{t})=5 \mathrm{~V}=1000\left(5-5 \mathrm{e}^{-2000 \mathrm{t}}-1.5\right) \mathrm{V}$
Solving for $t, t_{u p}=\ln [(3.5-.005) / 5] /(-2000)=179 \mu \mathrm{~s}$
$V_{I N, D N}(t)=5 e^{-2000 t} V \quad$ This input is going down from 5 V to 0 V . So will the output.
The output first hits 0 V at the very end of the linear region.
$\mathrm{V}_{\text {OUT }}(\mathrm{t})=0 \mathrm{~V}=1000\left(5 \mathrm{e}^{-2000 \mathrm{t}}-1.5\right) \mathrm{V}$
Solving for $\mathrm{t}, \mathrm{t}_{\mathrm{DN}}=\ln [1.5 / 5] /(-2000)=602 \mu \mathrm{~s}$

## Problem 2:

$$
P=4-\left(V_{I N}-2\right)^{2} W
$$

a) $\mathrm{V}_{\mathrm{IN}, \mathrm{BAD}}(\mathrm{t})=4 \mathrm{e}^{-\mathrm{t}} \mathrm{V}$

$$
\begin{aligned}
& E=\int_{t=0}^{\infty} P(t) d t=\int_{t=0}^{\infty} 4-(V \text { IN,BAD }(t)-2)^{2} d t=\int_{t=0}^{\infty} 4-\left(4 e^{-t}-2\right)^{2} d t=\int_{t=0}^{\infty}-16 e^{-2 t}+16 e^{-t} d t \\
& E=\left.\left(\frac{-16}{-2} e^{-2 t}+\frac{16}{-1} e^{-t}\right)\right|_{t=0} ^{\infty}=(0-8+0--16)=8 W
\end{aligned}
$$

b) Since $\mathrm{V}_{\mathbb{I N}, G O O D}(\mathrm{t})$ is the output of the comparator, it is either at the top rail voltage, in the linear region, or at the bottom rail voltage:
$\mathrm{V}_{\text {IN,GOOD }}(\mathrm{t})=\left\{\begin{array}{c}4 \mathrm{~V} \quad \text { when } 1000\left(\mathrm{~V}_{\operatorname{IN}, \operatorname{BAD}}(\mathrm{t})-1\right)>4 \\ 1000\left(\mathrm{~V}_{\text {IN }}, \operatorname{BAD}(\mathrm{t})-1\right) \quad \text { when } 0 \leq 1000\left(\mathrm{~V}_{\text {IN,BAD }}(\mathrm{t})-1\right) \leq 4 \\ 0 \mathrm{~V} \quad \text { when } 1000\left(\mathrm{~V}_{\operatorname{IN}, \operatorname{BAD}}(\mathrm{t})-1\right)<0\end{array}\right.$
When $\mathrm{V}_{\mathbb{I N , G O O D}}(\mathrm{t})=4 \mathrm{~V}$, the associated power, $\mathrm{P}=4-\left(\mathrm{V}_{\mathbb{I N , G O O D}}(\mathrm{t})-2\right)^{2}=0 \mathrm{~V}$.
When $\mathrm{V}_{\mathbb{I N}, \mathrm{GOOD}}(\mathrm{t})=0 \mathrm{~V}$, the associated power, $\mathrm{P}=4-\left(\mathrm{V}_{\mathbb{I N , G O O D}}(\mathrm{t})-2\right)^{2}=0 \mathrm{~V}$.

So the power absorbed is zero except when the comparator is in the linear region.
To complete the energy integral, we must find out when the comparator is in the linear region.

$$
\begin{array}{lll}
4 \mathrm{~V}=1000(\mathrm{~V} \operatorname{IN}, \operatorname{BAD}(\mathrm{t})-1) & 4 \mathrm{~V}=1000\left(4 \mathrm{e}^{-\mathrm{t}}-1\right) & \mathrm{t}=-\ln \left(\frac{1.004}{4}\right)=\ln \frac{4}{1.004} \\
0 \mathrm{~V}=1000\left(\mathrm{~V}_{\operatorname{IN}, \operatorname{BAD}(\mathrm{t})-1)}\right. & 0 \mathrm{~V}=1000\left(4 e^{-t}-1\right) & t=-\ln \left(\frac{1}{4}\right)=\ln 4
\end{array}
$$

Now compute the energy integral, knowing that $P(t)=0$ outside the linear region:

$$
\begin{aligned}
& E=\int_{t=0}^{\infty} P(t) d t=\int_{t=\ln \frac{4}{1.004}}^{\ln 4} 4-(V \operatorname{VIN}, G O O D(t)-2)^{2} d t=\int_{t=\ln \frac{4}{1.004}}^{\ln 4} 4-\left(1000\left(4 e^{-t}-1\right)-2\right)^{2} d t \\
& E=\int_{t=\ln \frac{4}{1.004}}^{\ln 4}-1004000-16000000 e^{-2 t}+8016000 e^{-t} d t \\
& E=\left.\left(-1004000 t-\frac{16000000}{-2} e^{-2 t}+\frac{8016000}{-1} e^{-t}\right)\right|_{t=\ln \frac{4}{1.004}} ^{\ln 4} \\
& E=\left(-1004000(\ln 1.004)+8000000\left(\frac{1}{16}-\frac{1.004^{2}}{16}\right)-8016000\left(\frac{1}{4}-\frac{1.004}{4}\right)\right)=10.6 \mathrm{~mW}
\end{aligned}
$$

So, cleaning up the signal before putting it into the digital circuit resulted in a lot less power consumption by the digital circuit!

## Problem 3:

There are many valid designs. In my design, I first use the inverting summer to multiply each individual binary digit by its place value. Then, I use an inverter to remove the negative sign, and divide by 4 since each binary 1 was 4 V and we want each 1 to represent 1 V in the output. The rails should be set to accommodate the maximum and minimum voltage that could come out of that op-amp.


## Problem 4:

When designing op-amp circuits, it's good to break the task at hand into smaller tasks. When converting from analog to digital, we have the following steps:

1. Determine if there is a " 1 " in the "twos" place. This means compare $\mathrm{V}_{\mathrm{IN}}$ to 2 V . Output logic $1(4 \mathrm{~V})$ in the "twos" place if higher, logic $0(0 \mathrm{~V})$ if lower.
2. Determine if there is a " 1 " in the "ones" place. This means:
a. Take $\mathrm{V}_{\mathbb{N}}$, and subtract off " 2 " if there is a " 1 " in the "twos" place. If there is not, subtract off " 0 ". This is getting rid of the "even" part of the number.
b. The result is what should be in the "ones" place. Compare the result to 1 V . If greater, output logic 1 in the "ones" place, else output logic " 0 ".

These smaller tasks can be implemented with op-amps. Many designs possible, here is one:


