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EECS 42 – Introduction to Electronics for Computer Science

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Solution to Problem Set # 10 (by Farinaz Koushanfar)

10.1

a) Gate 1: If (E1=0) → pull-down: ((A1.B1) + (C1.D1))' pull-up: (C1'+D1').(A1'+B1')
If (E1=1) → pull-down: ((B1+D1). (A1+C1))' pull-up: B1'.D1'+A1'.C1'
→ G1 = E1'. (C1'+D1').(A1'+B1')+E1. (B1'.D1'+A1'.C1')
(after simplification)→ G1 = A1'.C1'+B1'.D1'+E1'. (B1'.C1'+A1'.D1')

Gate 2: If (D2=0) → pull-down: (A2.B2)' pull-up: A2'+B2'
If (D2=1) → pull-down: (A2. (B2+C2))' pull-up: A2'+(B2'.C2')
→ G2 = D2'. (A2'+B2') + D2. (A2'+ (B2'.C2'))
(after simplification) → G2 = A2' + B2'. (C2'+D2')

b) As can be seen in the answer to part a), the functions of the pull-up and pull-down parts are complimentary, which makes sure that the pull-up and pull-down paths are not simultaneously on for any given input. Also, the pull-up circuit is all PMOS, and the pull-down is all NMOS. The complimentary feature also says that the pull-up and pull-down oaths are not "on" at the same time, so in the steady state, there is no current flowing from the source to the ground (the output is just connected to the source or to the ground).

c) For going from high to low in the output, the pull-down circuit should discharge the current. The pull-down delay of an inverter is: $\tau_{HL}(inv) = 0.69R_DC$.

Gate1: The minimum pull-down time occurs, when (A1=B1=C1=D1=1), $R_{eq}=2R_D||2R_D = R_D$
The max pull-down is when E1=1 and we have a path starting at one branch, and ending at the other, for e.g. (A1=E1=C1=1), $R_{eq}=3R_D$
Thus, the range $1 \le \tau_{HL}(gate1)/\tau_{HL}(inv) \le 3$.

Gate2: The minimum pull-down time occurs, when (A2=B2=C2=D2=1), $R_{eq}=5/3R_D$
The max pull-down is when (A2=C2=D2=1, B2=0), $R_{eq}=3R_D$
Thus, the range $1.66 \le \tau_{HL}(gate2)/\tau_{HL}(inv) \le 3$.

d) The pull-up delay of an inverter is: $\tau_{LH}(inv) = 0.69R_UC$

Gate1: The min pull-up happens when both pull-up branches are on (A1=B1=C1=D1=0), $R_{eq}=2R_U||2R_U = R_U$
The max pull-up is when there is only on path and that path passes E1 in the pull-up circuit, e.g. (A1=E1=D1=0, B1=C1=1). $R_{eq}=3R_U$.
Thus, the range is $1 \le \tau_{LH}(gate1)/\tau_{LH}(inv) \le 3$.

Gate2: The minimum pull-up time occurs, when (A2=B2=C2=D2=0), $R_{eq}= 0.6\ R_U$
The max pull-up is when (B2=C2=0, A2=D2=1), $R_{eq}=2R_U$
Thus, the range $0.6 \le \tau_{HL}(gate2)/\tau_{HL}(inv) \le 2$.

e) The overall worst-case delay for Gate1 is the $\max(\tau_{LH}(gate1),\tau_{HL}(gate1)) = 3\tau_{LH}(inv) = 3\tau_{HL}(inv)$
The overall worst-case delay for Gate2 is the $\max(\tau_{LH}(gate2),\tau_{HL}(gate2)) = 3\tau_{LH}(inv)$.

10.2

a) The best (or min) delay happens when the output of gate 2 is independent of the values of A2 (A2 is connected to output of gate 1) that happens when the circuit is pulled up with the other. So, if we assume that D2=C2=1 for a long time, and then the input B2 changes from 1 to 0, the delay for pulling up the output of the gate 2 becomes: $\tau_{LH}(gate2)$ for (B2=C2=D2=0), regardless of A2, which is $1.5\tau_{LH}(inv)$.

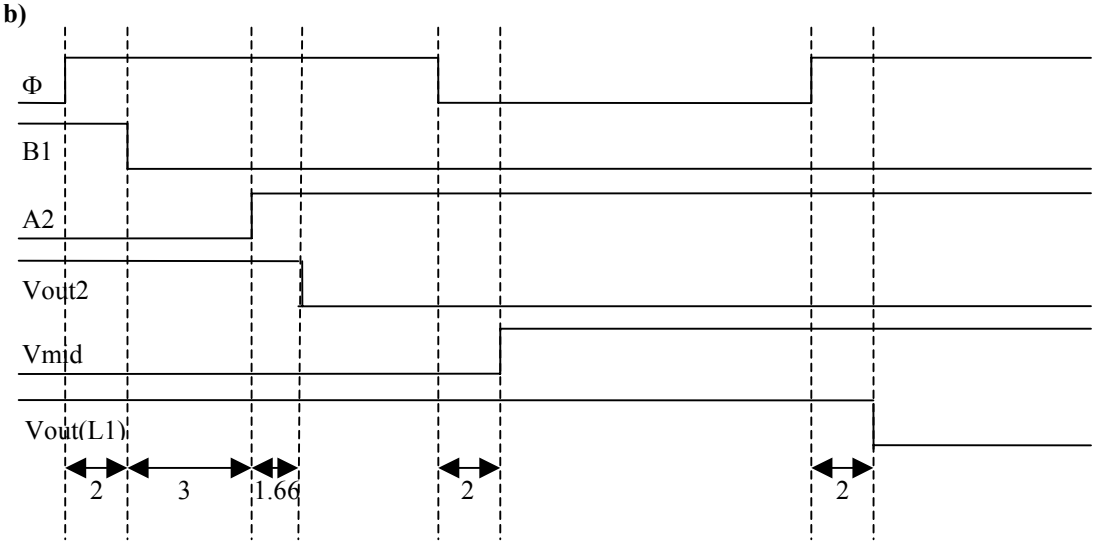
b) The longest propagation time is:
max(delay)/(inv delay)) = Max ($\tau_{HL}(gate1)/\tau_{HL}(inv) + \tau_{LH}(gate2)/\tau_{LH}(inv)$) = 3+3=6 (inverter delays)
Assume that (A1=B1=C1=D1=E1=0), then the inputs A1 and B1 change from 0 to 1, causing the worst case HL transition at the output of gate1 (3 inverter delays). Assume that the inputs (B2=D2=C2=1), then

the change in A2 (that is connected to the output of gate1 and goes to zero), will cause the worst case LH transition at the output of gate 2 (3 inverters delay).

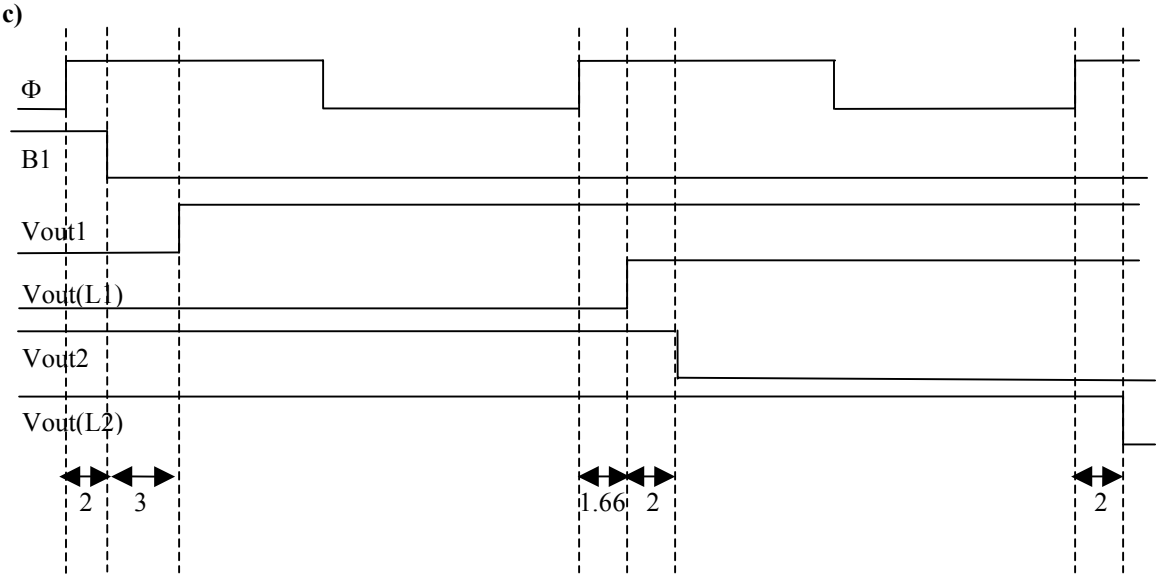
10.3

a) Each of the latches, consist of two stages. The first stage of the latch is transparent when the clock is low (Φ=0) and has the delay of ($0.69\times2\times R_DC$) or ($0.69\times2\times R_UC$) depending on if it is going from H to L or vice versa. The second stage of the latch is transparent when clock goes high, and has the delay of ($0.69\times2\times R_UC$) or ($0.69\times2\times R_DC$) depending on the transition. Overall, since the outputs of the two stages are compliment, the overall delay of a latch is: $(0.69\times2\times R_UC)+(0.69\times2\times R_DC) = 0.69\times2\times C(R_U+R_D)$, which is 4 inverter delays.

b)



c)



10.4

a) Once the clock goes from low to high,

- Time for the output of L0 to change = 2τ(inv)
- Worst case (max) for the output of gate 1 to change = 3τ(inv)
- Worst case (max) for the output of gate 2 to change = 3τ(inv)

When clock goes from high to low,

- Time for transferring the data in the mid-point of the latch = 2τ(inv)

Total (low to high) = 8 τ (inv), total (high to low) = 2τ(inv)

"Note that the total delay is dependent on the clock cycle, for all the cases we have here!"

b) For the first pipeline stage, once the clock goes from low to high,

- Time for the output of L0 to change = 2τ(inv)
- Worst case (max) for the output of gate 1 to change = 3τ(inv)
- Time for transferring the data in the mid-point of the latch L1= 2τ(inv)

Total (low to high) = 5 τ (inv), total (high to low) = 2τ(inv)

For the second pipeline stage, once the clock goes from low to high,

- Time for the output of L1 to change = 2τ(inv)
- Worst case (max) for the output of gate 2 to change = 3τ(inv)
- Time for transferring the data in the mid-point of the latch L2= 2τ(inv)

Total (low to high) = 5 (inv), total (high to low) = 2τ(inv)

c) The latency for the overall logic evaluation, (assuming the clock has τ_H(clock) and τ_L(clock))

For lumped logic = τ_H(clock) + τ_L(clock) = τ_H(clock) + τ_L(clock)

For pipelined logic = 2 (τ_H(clock) + τ_L(clock))

d) The lumped circuit (using the worst case calculations from 10.4(a)):

min {τ_H(clock)} = 8 τ (inv) min {τ_L(clock)} = 2 τ (inv)

The pipelined circuit (using the worst case calculations from 10.4(a)):

min {τ_H(clock)} = 5 τ (inv) min {τ_L(clock)} = 2 τ (inv)

Assuming minimum clock cycles, the overall delay of the G1 and G2 (for the output to be valid at the midpoint of last latch) is more with the pipelined circuit: 2 (τ_H(clock) + τ_L(clock)) = 14τ(inv) as opposed to the lumped circuit: τ_H(clock) + τ_L(clock) = 10τ(inv). However, if we just assume the delay of one cycle of the pipelined implementation, it has the minimum τ_H(clock) + τ_L(clock)=7τ(inv), which is 3τ(inv) faster than the lumped case, in terms of the clock cycle.