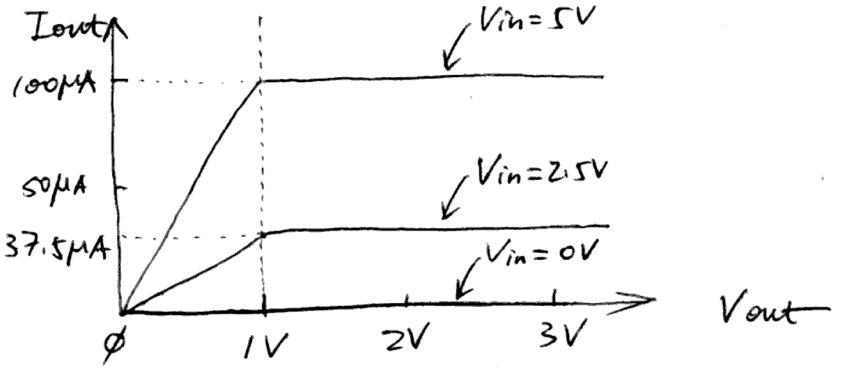
EE42 HW #9 Soln Yun Chiu

9.1 a)



b) $V_{out} = 0.5V > V_{out\_SAT\_D} = 1V$

$\Rightarrow$ xtor is in SAT region.

$\Rightarrow$ $I_{out} = K_D (V_{in} - V_{TO}) V_{out\_SAT\_D}$

$= 25\,\mu A/V^2 \times (3V - 1V) \times 1V$

$= 50\,\mu A$

c) $V_{out} = 0.5V < V_{out\_SAT\_D} = 1V$

$\Rightarrow$ xtor is in LIN region

$\Rightarrow$ $I_{out} = \frac{I_{out\_SAT\_D}}{2} = 25\,\mu A$

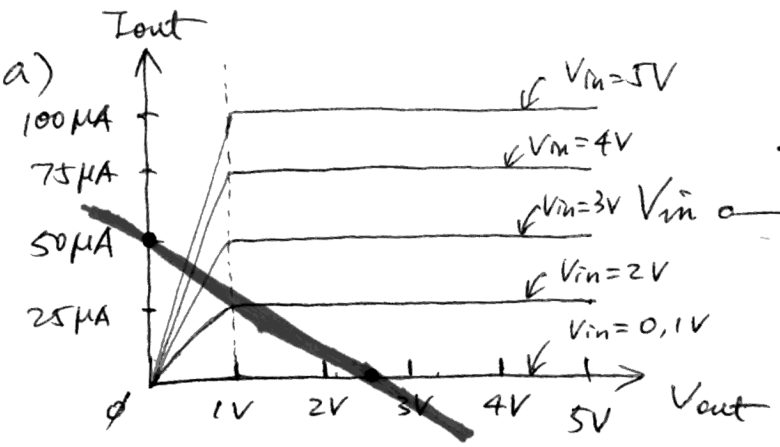
d) Same as c), but equivalent to find out V_{in} for $I_{out} = 30\,\mu A$ ($\because V_{out} = 0.5V = \frac{1}{2} V_{out\_SAT\_D}$)

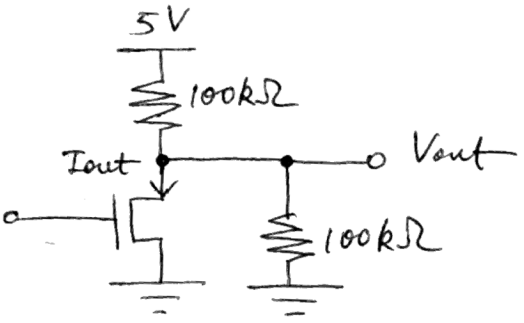
$\Rightarrow$ $30\,\mu A = 25\,\mu A/V^2 \times (V_{in} - 1V) \times 1V$

$\Rightarrow$ $V_{in} = 2.2V$

9.2

a)





9.2

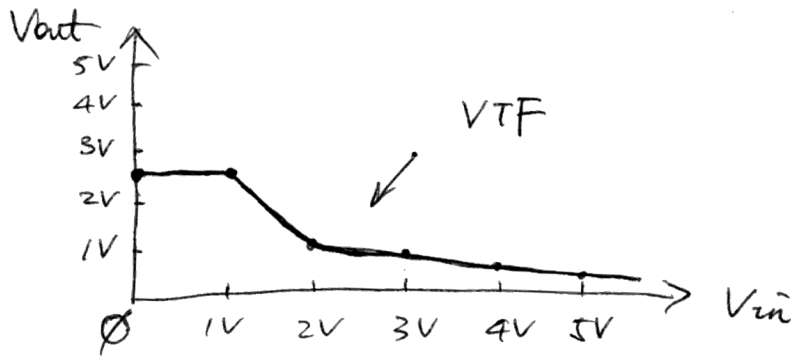
Caculate intercepts for the loadline of the resistors:

$$\begin{cases} I_{out} = \phi \Rightarrow V_{out} = \frac{100}{100+100} \times 5V = 2.5V \\ V_{out} = \phi \Rightarrow I_{out} = \frac{5V}{100k\Omega} = 50\,\mu A \end{cases}$$

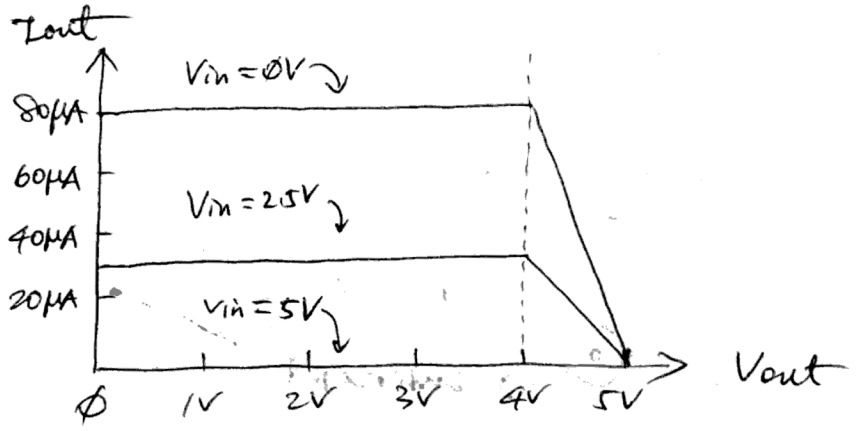
b) Read from the plot (approximately).

V_{in}	0V	1V	2V	3V	4V	5V
V_{out}	2.5V	2.5V	1V	0.7V	0.5V	0.4V

c)



9.3 a)



b) $V_{out} = 4.5V \Rightarrow$ Xtor is in LIN region.

$$I_{out} = \frac{I_{out\_SAT\_PD}}{2} = 20\mu A/V^2 \times (5V - 3V - 1V) \times 1V / 2$$

$$= 10\mu A$$

c) $V_{out} = 0.5V \Rightarrow$ Xtor is in SAT region.

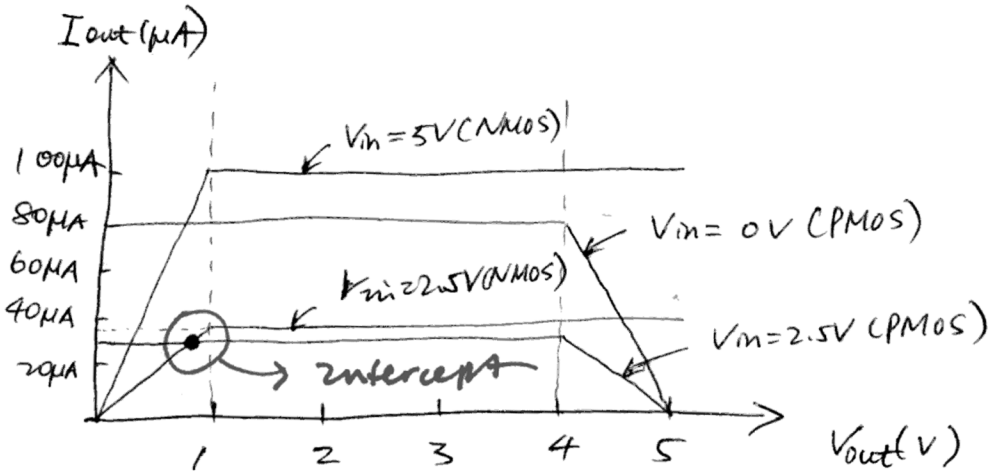
$$I_{out} = 20\mu A/V^2 \times (5V - 3V - 1V) \times 1V = 20\mu A$$

d) same as in c).

$$15\mu A = 20\mu A/V^2 \times (5V - V_{in} - 1V) \times 1V$$

$$\Rightarrow \quad V_{in} = 3.25V$$

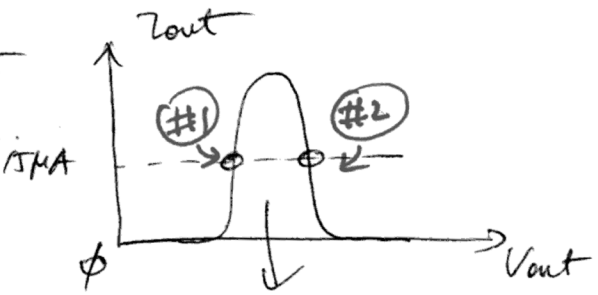
Q.4 a)



$V_M = 2.5V$, $I_{out} \approx 30\mu A$

$V_{out} \approx 0.8V$

b) Since CMOS inverter output current looks like a bell shape. There should be 2 solns possible for this question.



2 solns possible

(#1) NMOS SAT, PMOS LIN.

$\Rightarrow$ NMOS determine current.

NMOS: $15\mu A = 25\mu A\,(V_{in}-1) \Rightarrow V_M = 1.6V$

PMOS: $15\mu A = 20\mu A\,(5-1-V_{in})\cdot(5-V_{out}) \Rightarrow V_{out} = 4.6875V$

(#2) NMOS LIN, PMOS SAT.

NMOS: $15\mu A = 25\mu A\,(V_M-1)\,V_{out} \Rightarrow V_{out} = 0.2667V$

PMOS: $15\mu A = 20\mu A\,(5-1-V_M) \Rightarrow V_M = 3.25V$

c) Since NMOS pull-down is stronger than PMOS pull-up, V_M has to be less than 2.5V. So PMOS must be in SAT region. Assume NMOS is also in SAT.

$$\Rightarrow I_{out} = I_{NMOS} = 25\mu A\,(V_M-1) \Rightarrow V_M = \frac{7}{3}V$$
$$= I_{PMOS} = 20\mu A\,(5-V_M-1)$$

Note: Double check our assumption validity.

d)