

EECS 42 – Introduction to Electronics for Computer Science



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Dept. EECS, 510 Cory
UC Berkeley
Course Web Site

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Problem Set # 10 Due 4:30 PM April 30th, 240 Cory

Reading: Week 13# Diodes and MOS Devices, S&O 13.1-13.2, 518-526.

This is an easy but instructive problem set to walk you through data dependent propagation delays and the maximum clock frequency.

Use the circuits for Gate1 and Gate2 below. Throughout this problem make the simplifying assumption that each gate or latch stage has a load of 50 fF and that each 'on' transistor has a resistance of 10k Ω . That is $R_D = R_U = 10 \text{ k}\Omega$. The inverter delay is $0.69(10\text{k}\Omega)50\text{fF} = 345 \text{ ps}$.

10.1 Data Dependence of Single-Gate Delay.

- Determine the logic function of Gate1 and Gate2.
- Describe 3 features that combine together to make these gates complementary.
- Find the minimum and maximum propagation delay τ_{HL} for the output going from high to low for each of the gates. Give the data dependent range of delays compared to a simple inverter (such as $\frac{1}{2}$ to $\frac{7}{3}$ the inverter delay).
- Find the minimum and maximum propagation delay τ_{LH} for the output going from low to high for each of the gates. Give the data dependent range of delays.
- Give the worst case over-all range of data dependent delays.

10.2 Data Dependence of Cascade-Gate Delay. For this problem assume that the output of Gate1 is connected to the input A2 of Gate2 and that the capacitive loads remain unchanged.

- Determine the shortest propagation delay for the output of Gate2 to change compared to an inverter and give a set of initial inputs and input changes that produce it.
- Determine the longest propagation delay for the output of Gate2 to change compared to an inverter and give a set of initial inputs and input changes that produce it.

10.3 Lumped vs. Pipelined Logic. Latches are now introduced to synchronize transfer of logic outputs among circuits as shown below. There are two implementations. In the lumped implementation the cascade of Gate1/Gate2 from 10.2 is placed after a latch L0 that releases B1 and the cascade circuit is followed by and output hold latch L1. In the pipelined implementation the latch L0 that releases B1 is followed first by Gate1 alone, then an output hold latch L1, then Gate2 and finally an output hold latch L2. Assume that the inputs have been $A1 = 1, B1 = 1, C1 = 0, D1 = 1, E1 = 0, A = V_{OUT1}, B2=1, C2 = 1, D2 = 1$ for a long time. However, prior to the rising edge of the clock at $t = 0$, the first stage in L0 has permanently gone high so that on the rising edge B1 starts its transition to 0.

- Determine the propagation delay of the latch circuit for both the rising edge and falling edge of the clock in units of inverter delay.
- Sketch the output of Gate1 (V_{OUT1}) and the output of Latch1 (V_{LATCH1}) versus time in the timing diagram for the lumped implementation. (Assume clock goes up for 10 inverter delays and then down for 10 inverter delays).
- Sketch the output of Gate1 (V_{OUT1}), the output of Latch1 (V_{LATCH1}), the output of Gate2 (V_{OUT2}), the output of Latch2 (V_{LATCH2}) versus time in the timing diagram for the pipeline implementation using the clock from b).

10.4 Latency and Throughput of Lumped and Pipelined Logic.

- Determine the maximum data dependent latch-to-latch delay of the lumped implementation. This is the time from the rising clock edge on the input release latch L0 until the next possible rising clock edge. That is the output of L0 must change, the Gate1

must react, Gate2 must the react and finally the clock must go low long enough for latch L1 input stage to react. (Hint: Add the delays in clock high and those in clock low.)

- Determine the maximum data dependent latch-to-latch delay of each sub-section of the pipeline implementation.
- The latency of the overall logic evaluation is the time for the data to appear on the final output latch. Find the latency for the lumped and pipeline implementations in terms of a number of inverter delays. (Be sure to use the output of L2 for the pipeline).
- The minimum clock period must be larger than the maximum latch-to-latch delay. The maximum clock frequency is the inverse of the minimum clock period. Find the minimum clock period for the lumped and pipelined implementations. The clock need not go low for as long as it goes high. Assuming one computed result comes out per clock cycle, how much faster is the pipeline architecture than the lumped architecture?

