EECS 42 – Introduction to Electronics for Computer Science

Spring 2003, **Prof. A. R. Neureuther**
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Problem Set # 9 Due 2:30 PM April 9th, 240 Cory

Reading: Week 10# Logic with State Dependent Devices S&O 593-595,604-611 (read for graphs and not device equations) plus Handouts lectures 16 and 17.

9.1 NMOS I versus V. Use the 42S_NMOS equation from Lecture 16.

a) Sketch I_{OUT} versus V_{OUT} for V_{IN} = 0, 2.5 and 5 V.
b) Find I_{OUT} when V_{IN} = 3.0V and V_{OUT} = 4.5V.
c) Find I_{OUT} when V_{IN} = 3.0V and V_{OUT} = 0.5V.
d) Find V_{IN} when I_{OUT} = 15 μA and V_{OUT} = 0.5V.

9.2 Logic Gate with a resistive load. Use the 42S_NMOS equation from Lecture 16 and assume that a logic gate has a 100kΩ pull-up resistor to V_{DD} = 5V. In addition, assume that the output of the gate is loaded by a second 100kΩ resistor to ground. (The final circuit is like that in the last slide in Lecture 16 but the 200kΩ resistor is now a 100kΩ resistor.)

a) Draw the load line for this circuit on the I_{OUT} versus V_{OUT} of Problem 9.1.
b) Find V_{OUT} for V_{IN} = 0, 1, 2, 3, 4, and 5V.
c) Sketch the voltage transfer characteristic for this loaded circuit.

9.3 PMOS I versus V. Use the 42S_PMOS equation from Lecture 17.

a) Sketch I_{OUT} versus V_{OUT} for V_{IN} = 0, 2.5 and 5 V.
b) Find I_{OUT} when V_{IN} = 3.0V and V_{OUT} = 4.5V.
c) Find I_{OUT} when V_{IN} = 3.0V and V_{OUT} = 0.5V.
d) Find V_{IN} when I_{OUT} = 15 μA and V_{OUT} = 0.5V.

9.4 CMOS Operation. A 42S_NMOS and a 42S_PMOS device to form an inverter with V_{DD} = 5V as discussed in Lecture 17. Use your results from 9.1 and 9.3 to help you do the following.

a) On the same axes, draw I_{OUT} vs V_{OUT} for the NMOS and PMOS when connected as a CMOS circuit with V_{IN} = 2.5V and find the intersection point (I_{OUT}, V_{OUT}).
b) Find V_{OUT} for the CMOS circuit when I_{OUT} = 15 μA. {Hint: You can not directly combine 9.1 d) with 9.3 d). Instead choose the one of these two for which the current is in saturation and locally independent of V_{OUT} to first find V_{IN}. Then, use this V_{IN} to find a new V_{OUT} for the device that is not in saturation.}
c) Find V_M (or V_{MID})
d) Sketch the VTC for this circuit.