Lecture 28

CMOS LOGIC

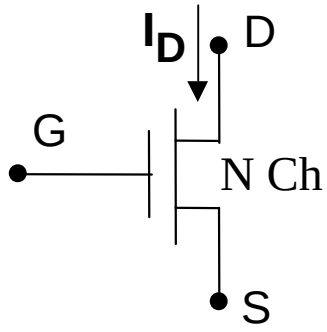
Lectures 21:

- NMOS Switching Model
- PMOS Switching Model
- CMOS inverter and Switching Model

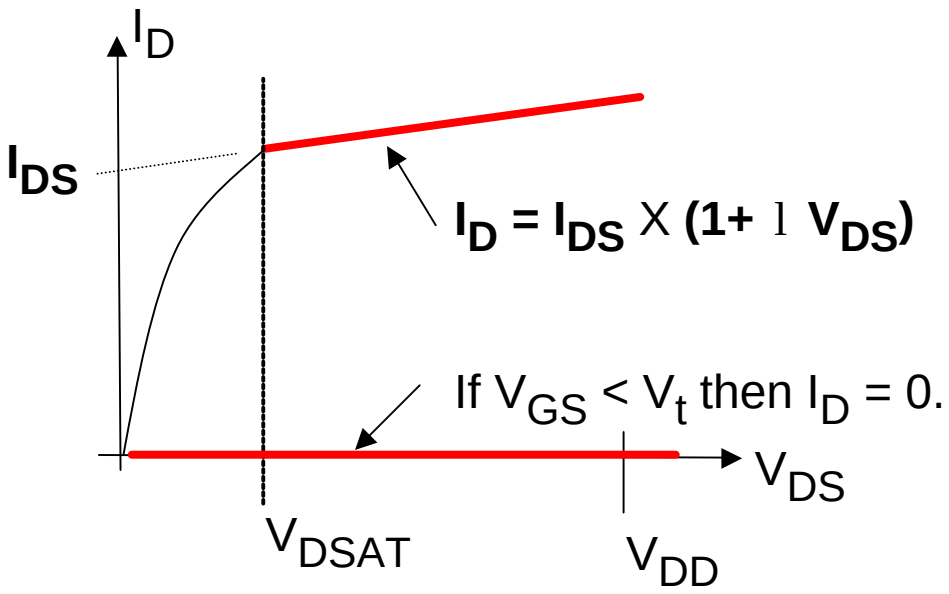
TODAY:

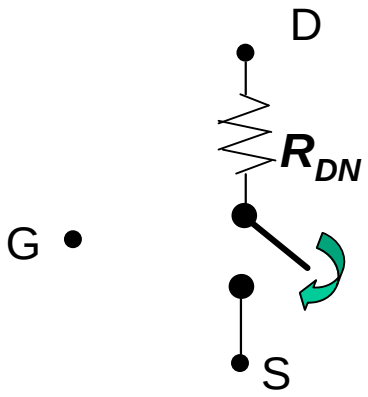
- CMOS Logic Gates: NAND, NOR
- Delay in Inverters and Logic Gates
- Top view of layout

NMOS Switching Summary



The circuit symbol



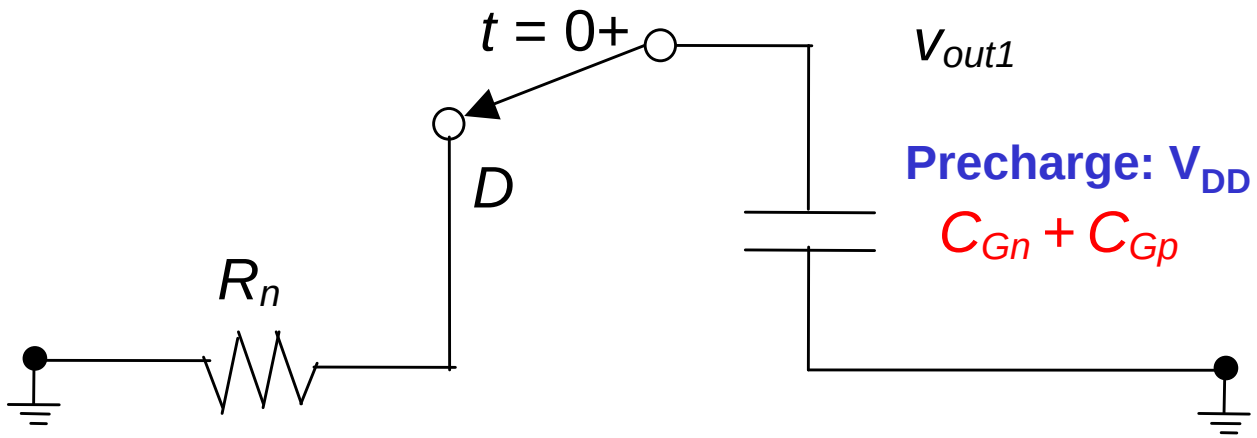


Electrical Model

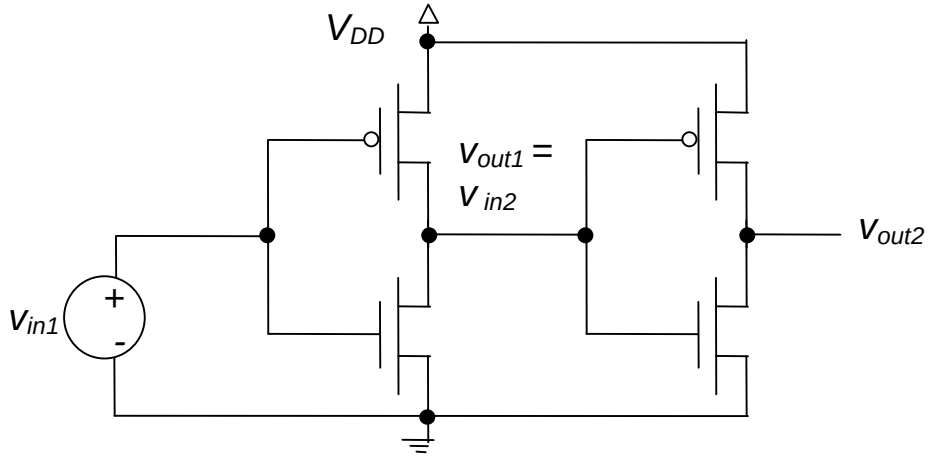
How is the effective resistance (R_{DN}) for RC calculations of switching time related to the I-V graph?

Pull-Down Operation

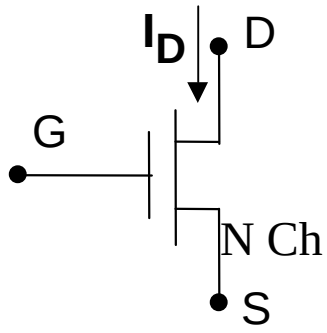
The job of R is to pull down the capacitance from its initial voltage of V_{DD} to V_{DD} /2. And at almost constant current (= I_{DS}).



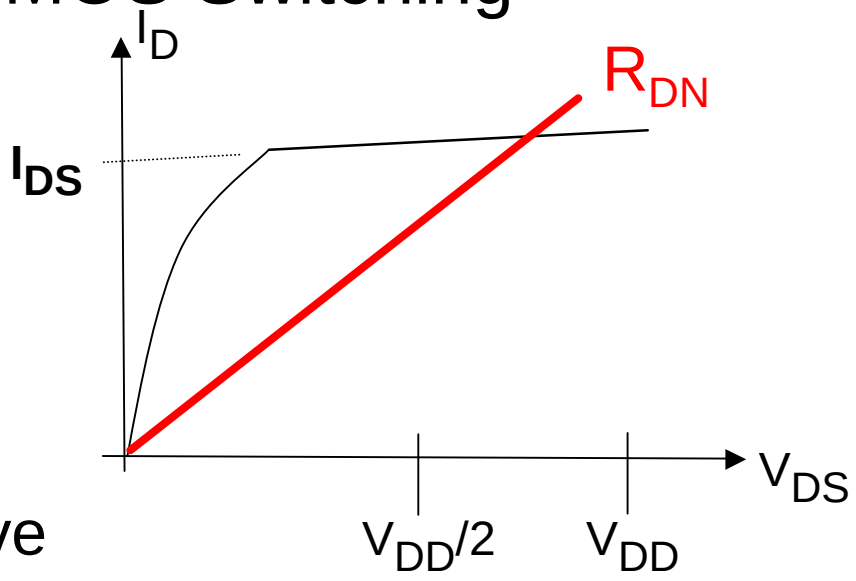
As you found in Home Prob Set 13 you can use I_{DS} = CdV/dt to find the time Dt.



NMOS Switching



The circuit symbol



From $I_{DS} = CdV/dt$ we have

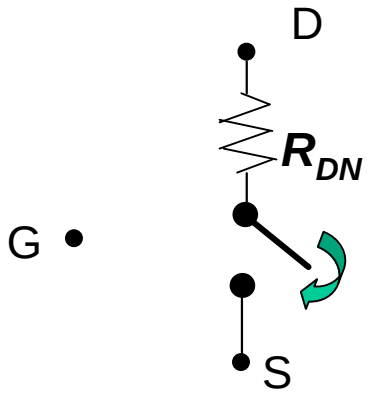
$\Delta t = C\Delta V / I_{DS} = C V_{DD} / 2 I_{DS}$

But if we had an RC discharge

$\Delta t = 0.69RC$ so the effective resistance, R_{DN} ,$= \Delta t / 0.69C$

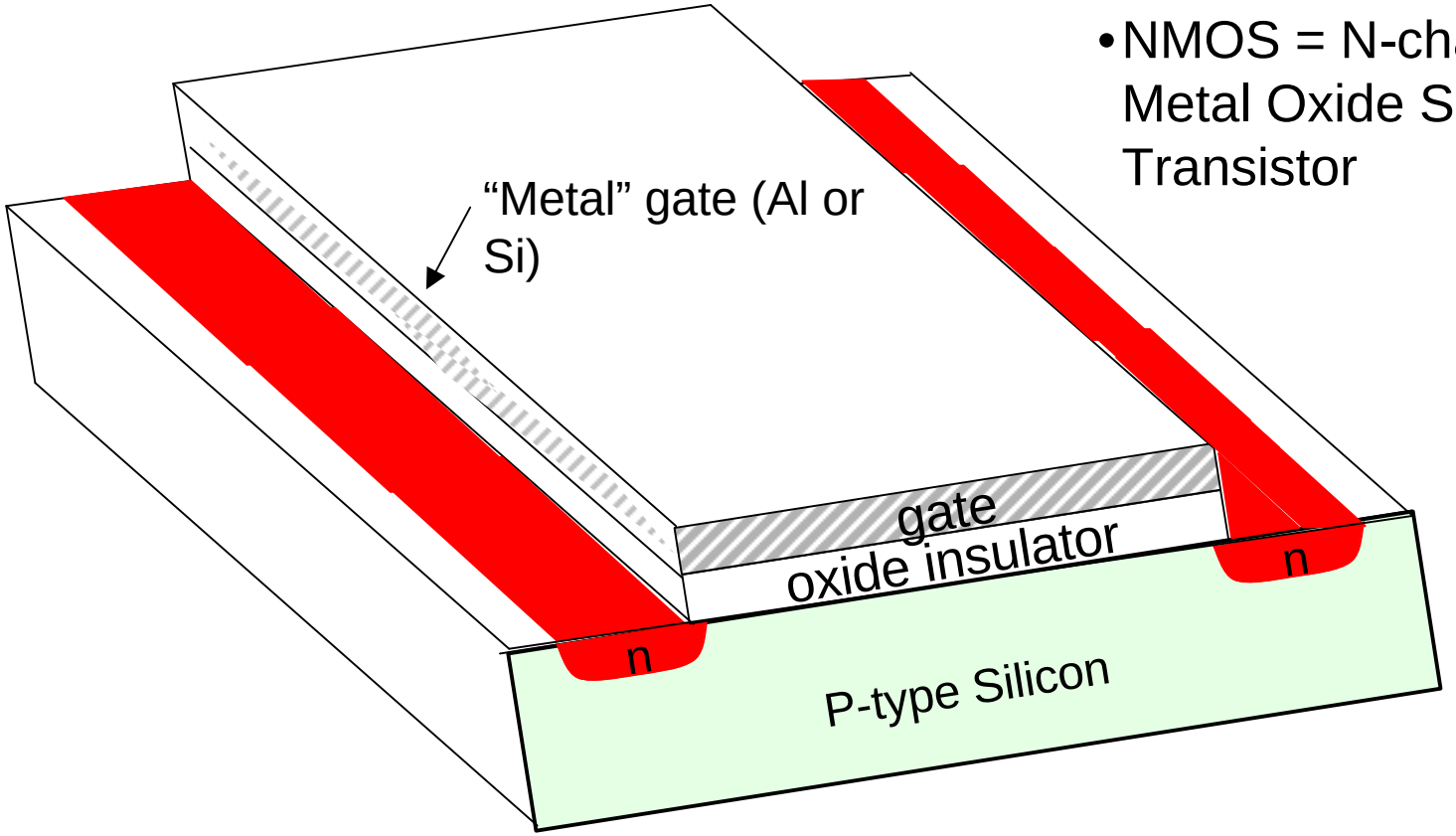
$= V_{DD}/(0.69 \text{ X } 2 I_{DS}) = .72 V_{DD} / I_{DS}$

So we use $$R_{DN} \approx \frac{3}{4}\frac{V_{DD}}{I_{DS}}$$



Electrical Model

NMOS TRANSISTOR STRUCTURE

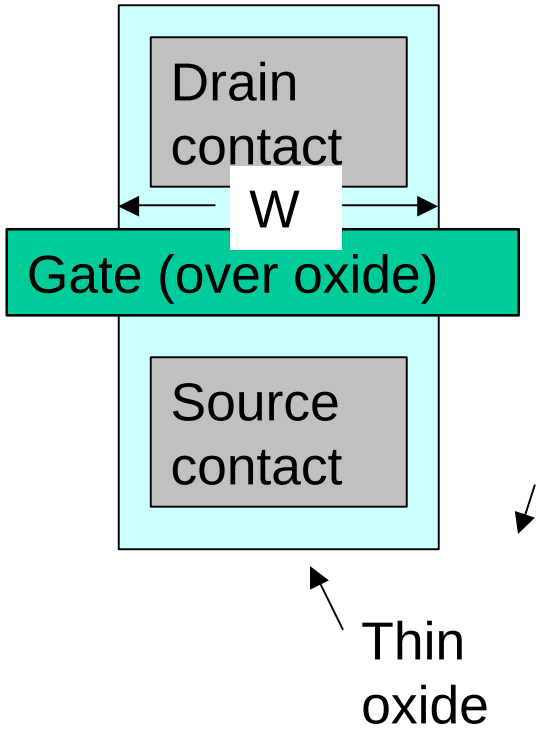


- NMOS = N-channel Metal Oxide Silicon Transistor

- The key elements of the layout are a source and drain region, a thin oxide region and a gate.

  - Lets look at a top view of how a device might be drawn

MOS LAYOUT



What are device dimensions?

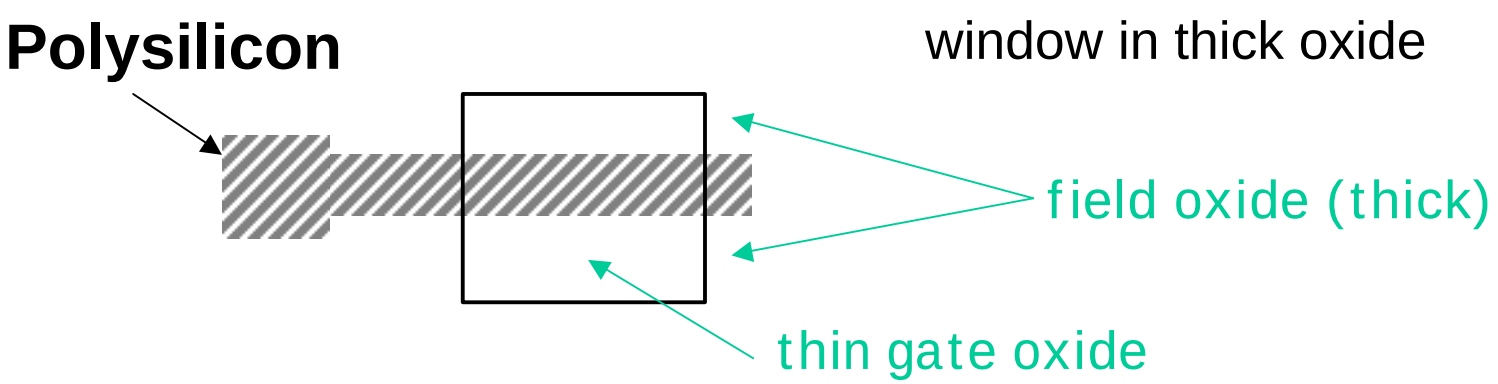
Gate Length = L

Gate Width = W

Gate Area (for capacitance) is W x L (because that is the thin oxide area covered by the gate)

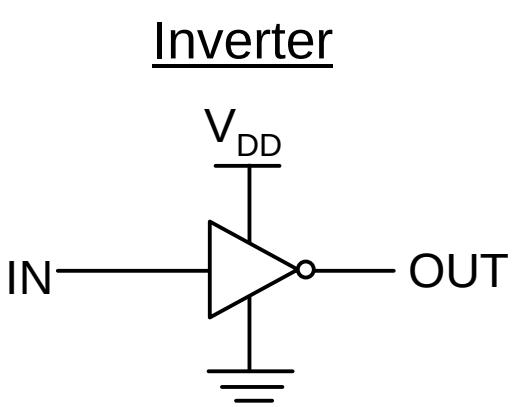
MOSFET "Identification"

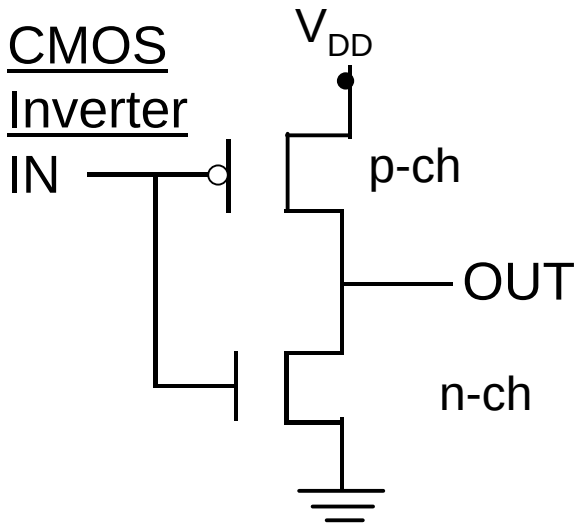
Poly line crossing a thin oxide region → MOSFET

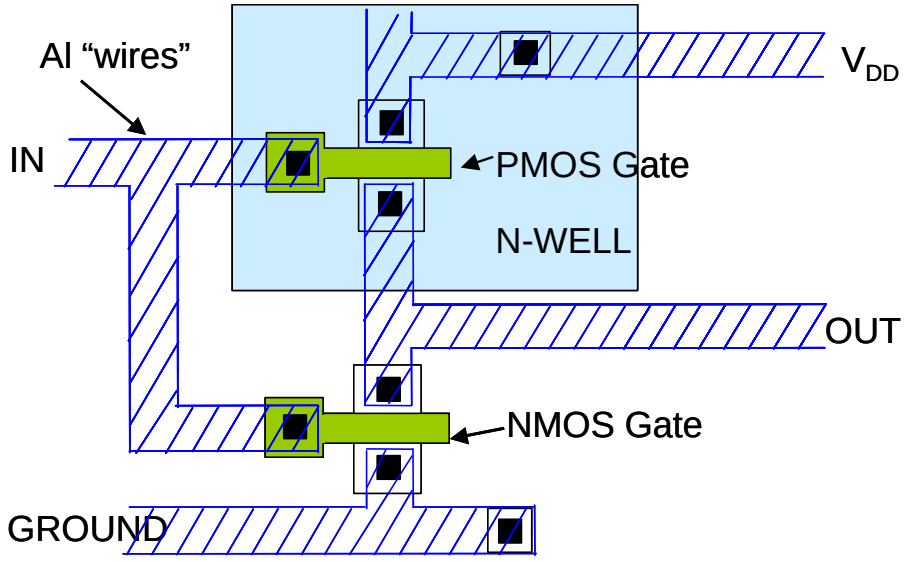


Is oxide region inside the n-well? If Yes, then PMOS; If No, then NMOS

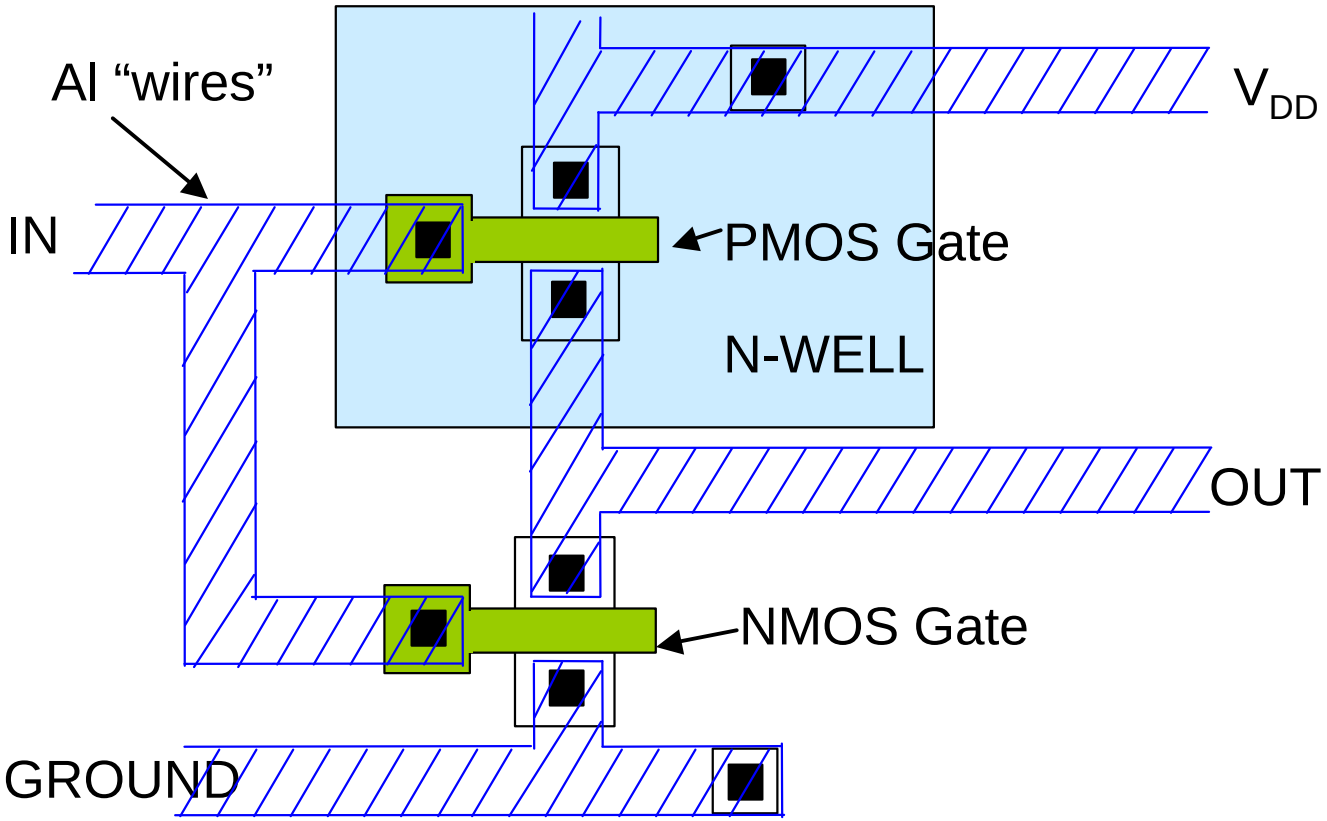
Basic CMOS Inverter







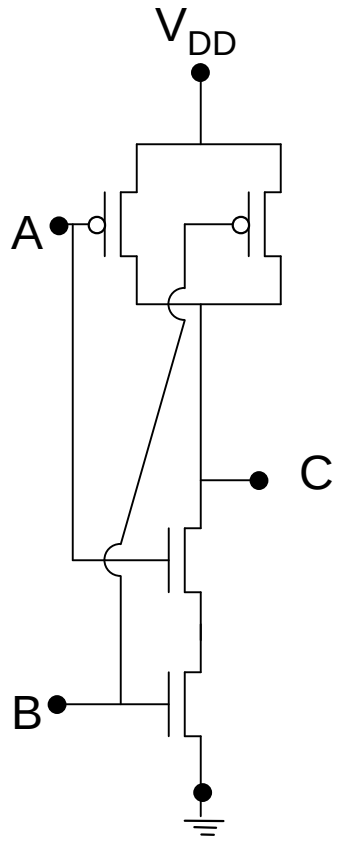
Example layout of CMOS Inverter


Al “wires”
V_{DD}
IN
PMOS Gate
N-WELL
OUT
NMOS Gate
GROUND

CMOS DIGITAL LOGIC

NAND gate

A	B	A B	C= $\overline{A\,B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0



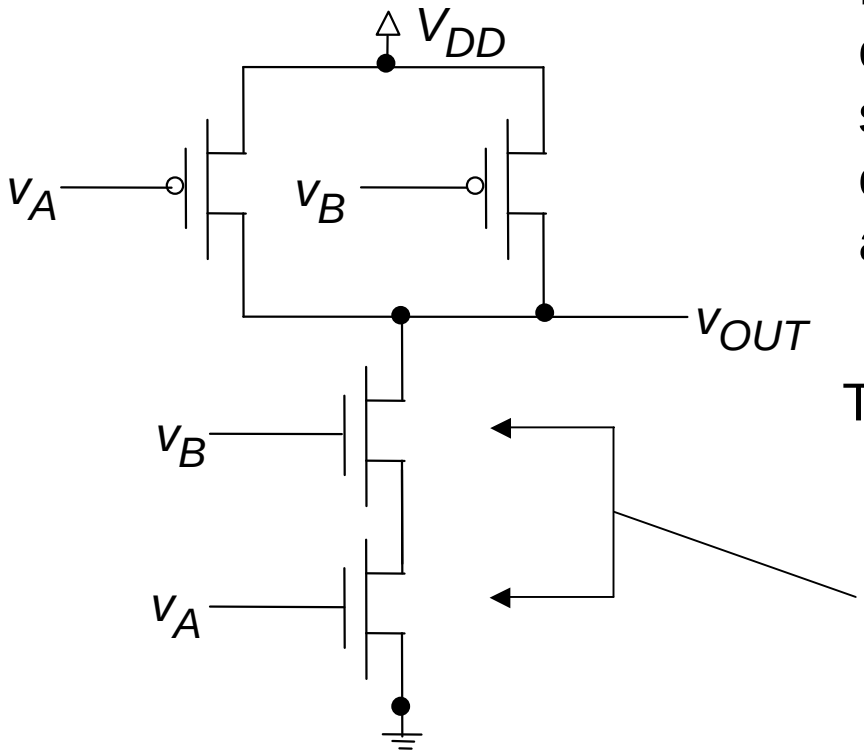
Making a NAND gate:

NMOS portion: both inputs need to be high for output to be low → series

PMOS portion: either input can be low for output to be high → parallel

CMOS NAND GATE

NMOS switches in series from output to ground; PMOS switches in parallel from output to the supply (Here we left out the A-A and B-B connection for clarity)

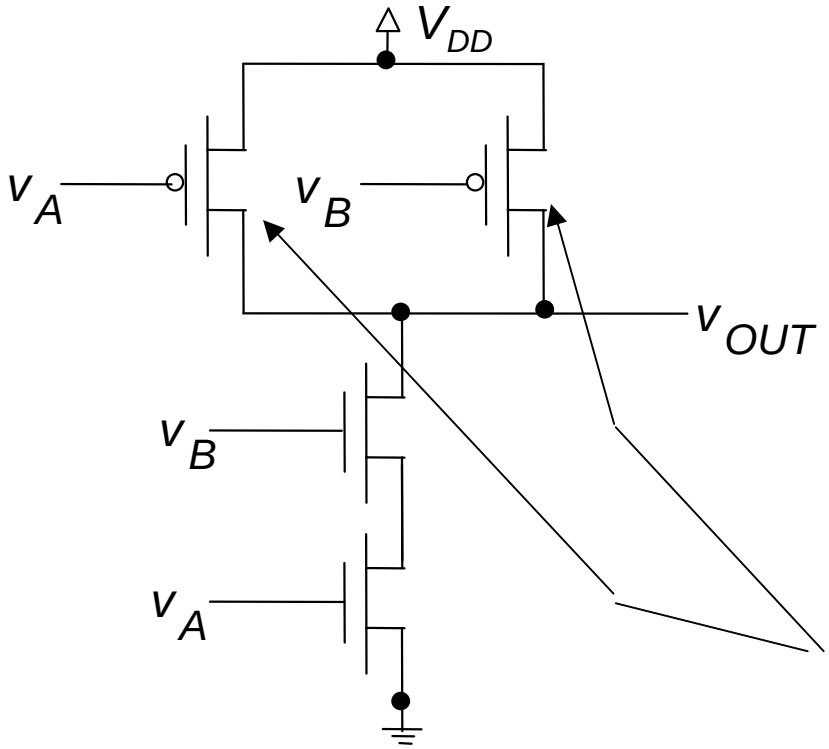


NAND: If *either* output is low then one of the bottom (pull down) series switches is open and one of the upper (pull up) switches are closed.

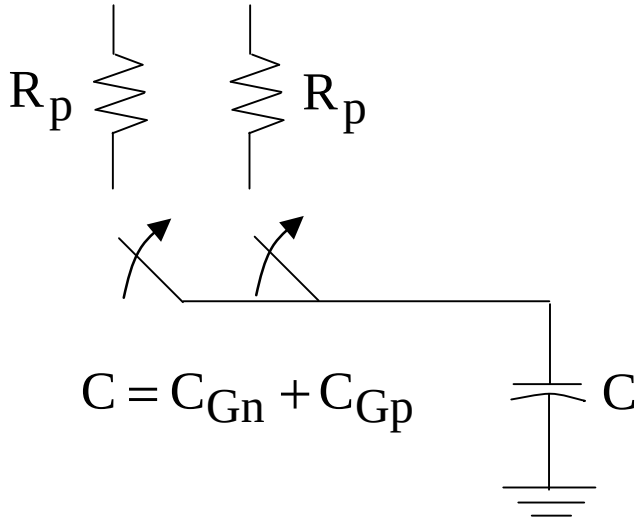
Thus the output is pulled high.

Behaves like 2 R_n's in series when both A and B are high

NAND Gate Pull-Up Model*



$\Rightarrow$

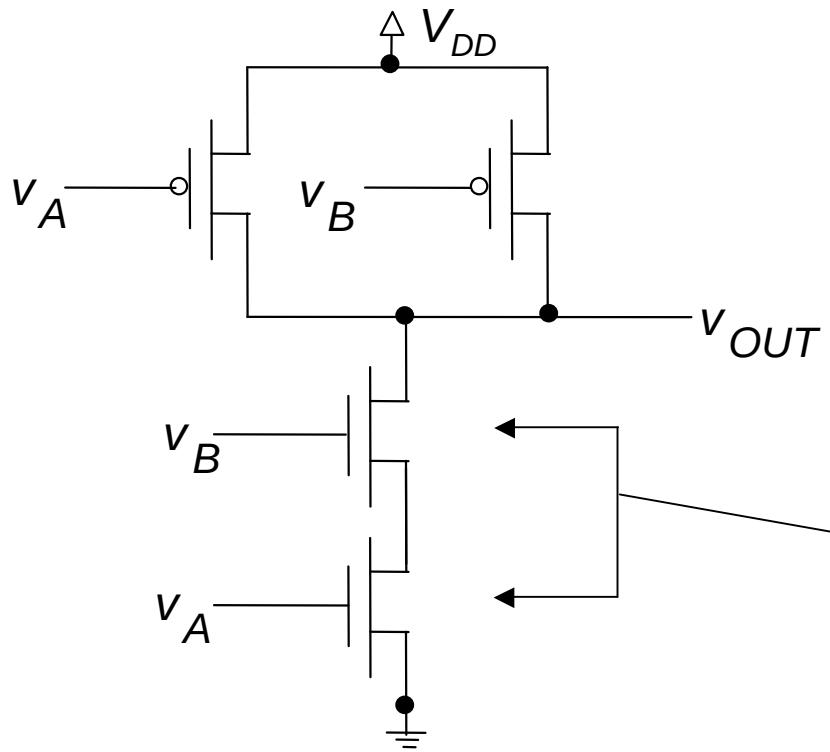


One or both switches closed
(worse case: one switch)

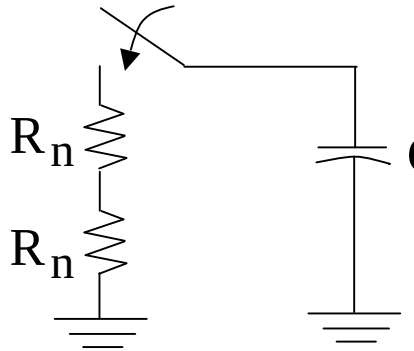
$$\tau = RC = R_pC \quad = R_p(C_{Gn} + C_{Gp})$$

* For first-order analysis we consider only gate capacitance.
Remember: we must add drain and interconnect for accurate estimates.

NAND Gate Pull-Down Model*



$\Rightarrow$



$C = C_{Gn} + C_{Gp}$

Two R_n's add in series, so RC = $2R_nC = 2R_n (C_{Gn} + C_{Gp})$

If $2R_n \sim R_p$, this circuit is balanced for equal rise and fall times.

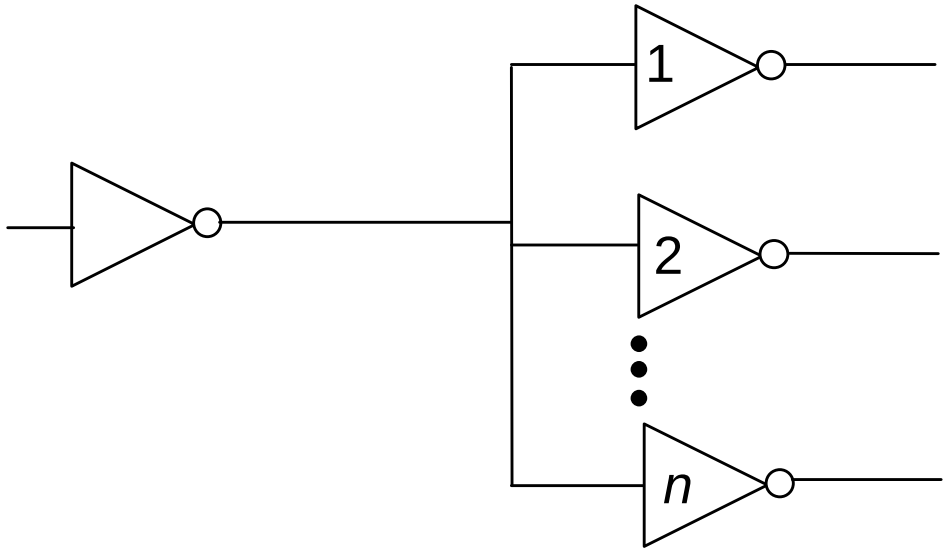
* For first-order analysis we consider only gate capacitance.

LOADS

We have been considering a single gate as load. But in real designs the output of one gate may drive many gates. We call the number of driven gates the *Fanout.*

Definition of Fanout

Fanout = number of gates that are connected to the driver

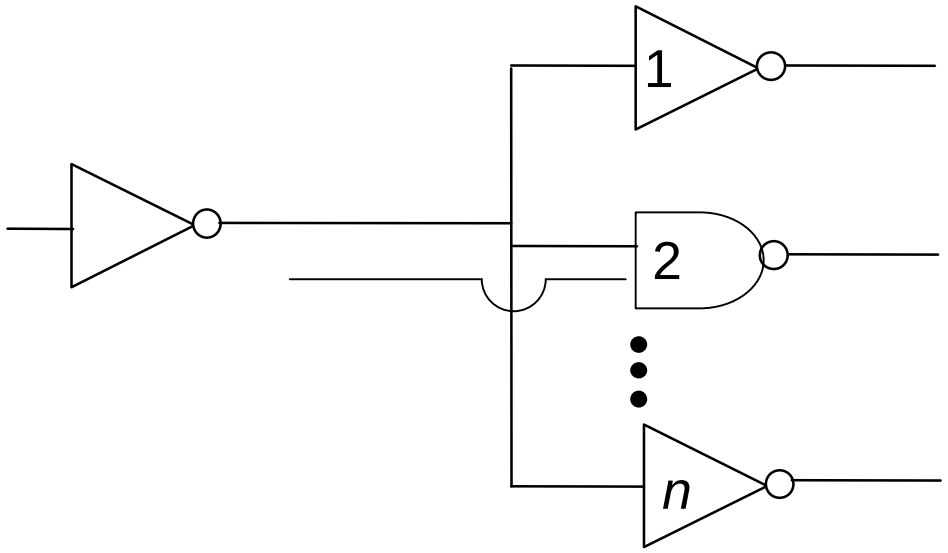


Fanout leads to increased capacitive load (and higher delay)

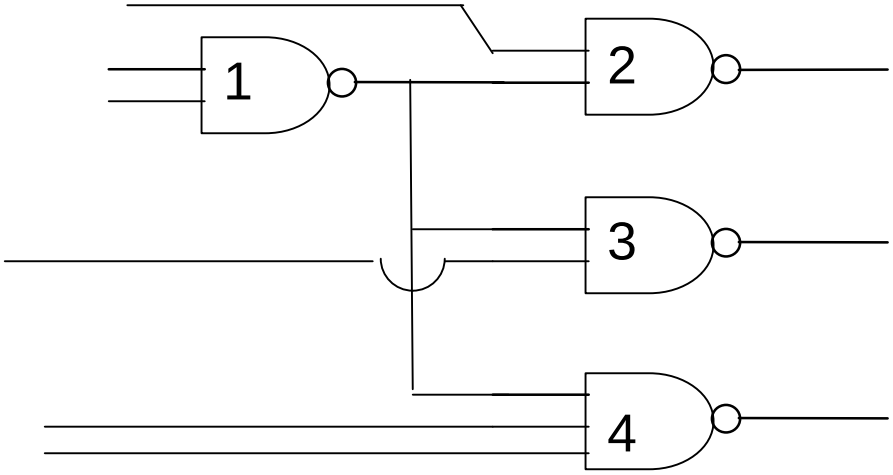
Fanout

Fanout is always ≥ 1 (there is always a load)

Gate capacitances sum and are charged by the driver resistance



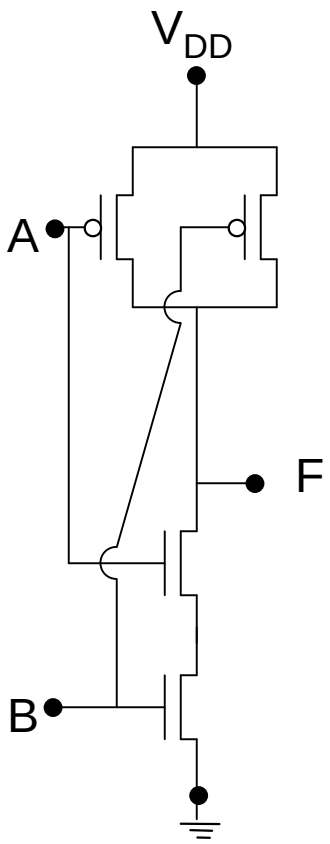
Fanout



NAND gate 1 drives the inputs to 2 one-input NAND gates and one 3-input NAND gate

What capacitance does the output of NAND gate 1 drive?

NAND Gates

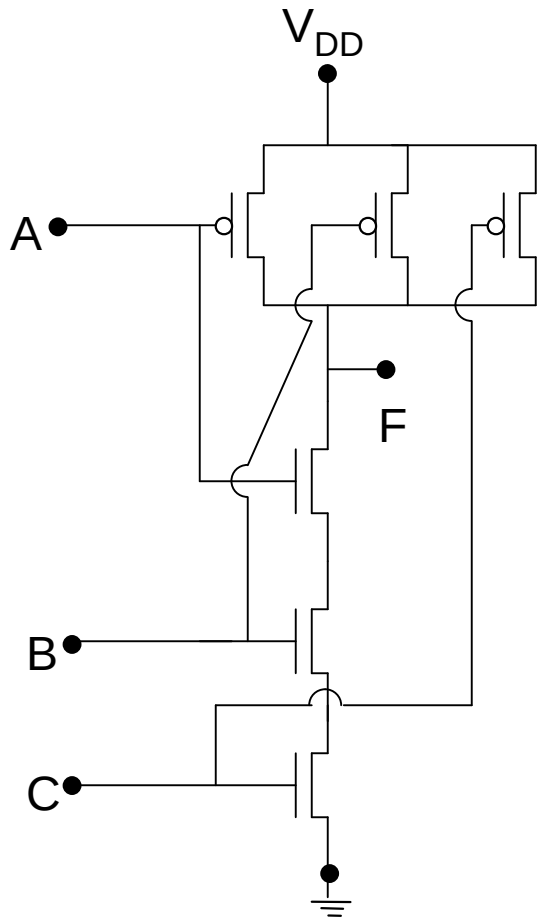


2-input NAND

Each input loads with $C_{GN} + C_{GP}$

Output drives with $2R_{DN}$ or R_{DP}

For examples see
Problem set 14



3-input NAND

Each input loads with $C_{GN} + C_{GP}$

Output drives with $3R_{DN}$ or R_{DP}