Lecture 27/28

Last time:

NMOS = n-channel Metal Oxide Semiconductor Field Effect Transistor

CMOS is a process that uses both NMOS and PMOS devices (complementary)

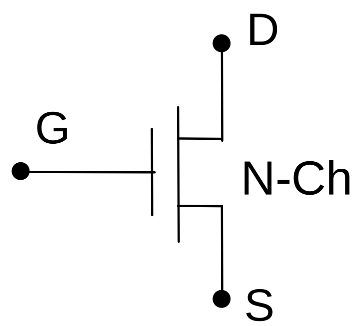
NMOS and PMOS Switch Models

Today -

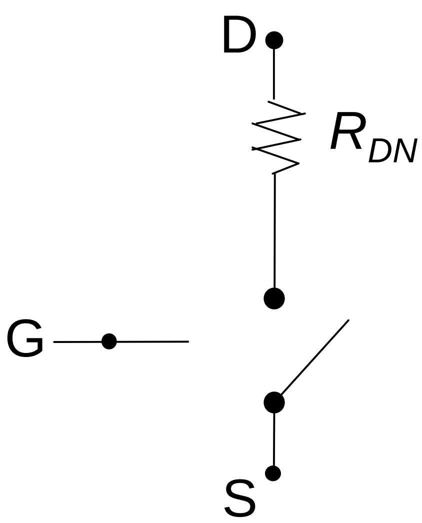
- NMOS and PMOS models including Capacitance
- CMOS inverter electrical behavior
- Glimpse of layout (more next time)

NMOS Circuit Model

NMOS transistor has an equivalent resistance R_{DN} when closed



The circuit symbol



The Switch model

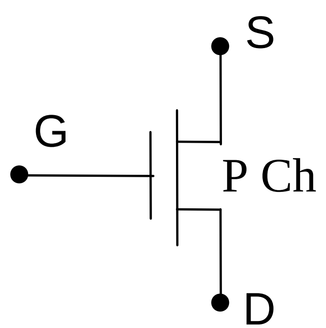
NMOS SWITCH

- If $V_{GS} \approx 0$, Switch is open
(e.g. $V_S = 0$, $V_G = 0$.)

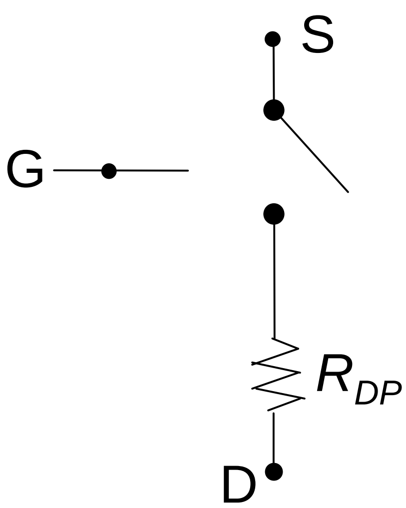
- If $V_{GS} >> V_T$, Switch is closed
(e.g. $V_S = 0$, $V_G = V_{DD}$.)

PMOS Circuit Model

PMOS transistor has an equivalent resistance R_{DP} when closed



The circuit symbol



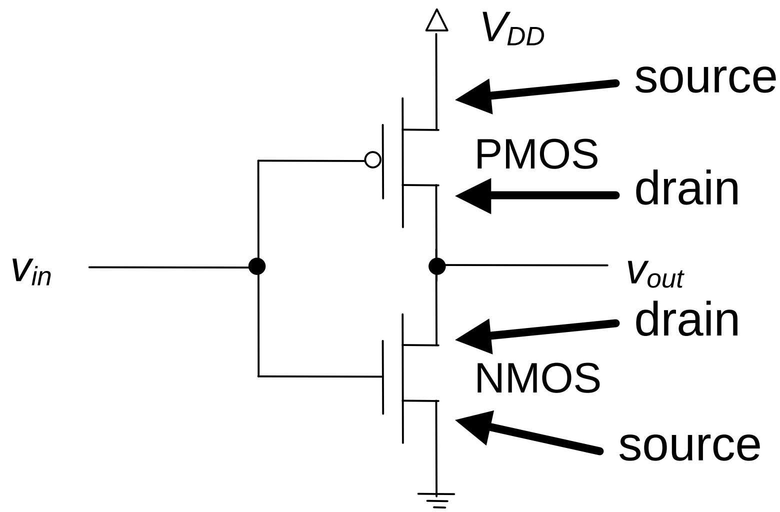
The Switch model

PMOS SWITCH

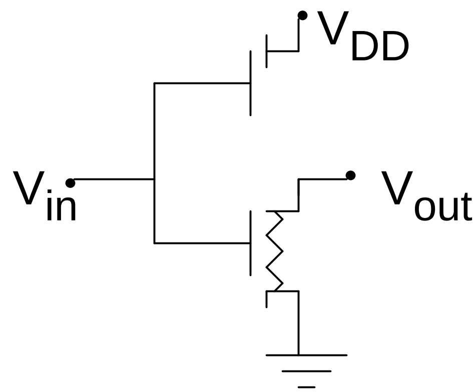
- If $V_{GS} \approx 0$, Switch is open (e.g. $V_S = V_{DD}$, $V_G = V_{DD}$.)

- If $|V_{GS}| >> |V_T|$, Switch is closed (e.g. $V_S = V_{DD}$, $V_G = 0$.)

THE BASIC STATIC CMOS INVERTER

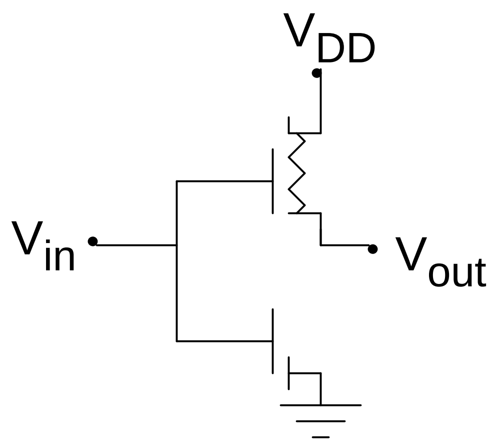


For V_{in} > 1.5V NMOS on , PMOS off



V_{out} **= 0**

For V_{in} < 1V NMOS off , PMOS on



$V_{out} = V_{DD}$

Example for Discussion:

NMOS: V_{Tn} = 1V

PMOS: V_{Tp} = -1V

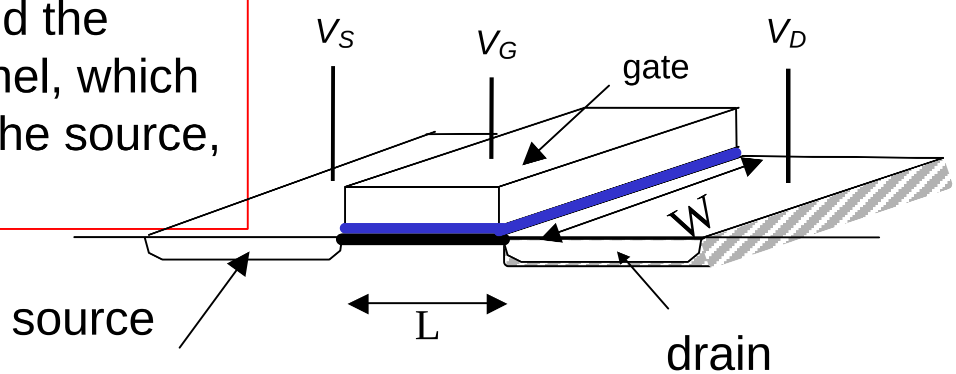
Let V_{DD} = 2.5V

Model Refinements: Add Gate Capacitances

Node connected to the gate:

Capacitance C_G is between gate and the underlying channel, which is connected to the source, $C_{GS} = C_G$

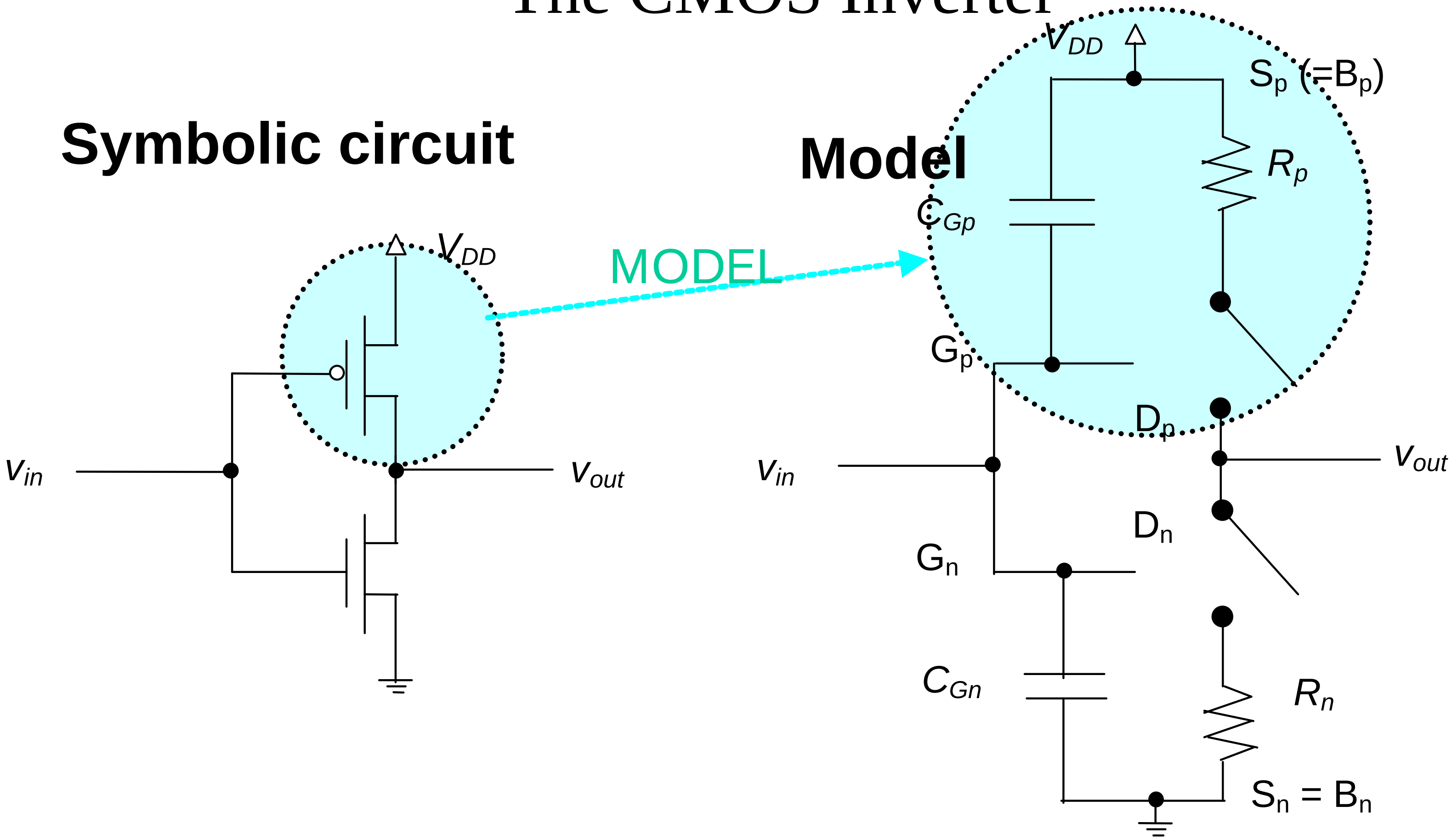
$$C_G = C_{ox} \times W \times L = \frac{e_{ox} WL}{t_{ox}}$$



The gate capacitance is the dominant capacitance, perhaps 60-80% of total node capacitance. So we will focus just on it.

To compute it we need the gate capacitance per unit area (e_{ox}/t_{ox}) and the gate area (W x L).

The CMOS Inverter



Note that the switches are NOT independent , in fact they are “ganged”

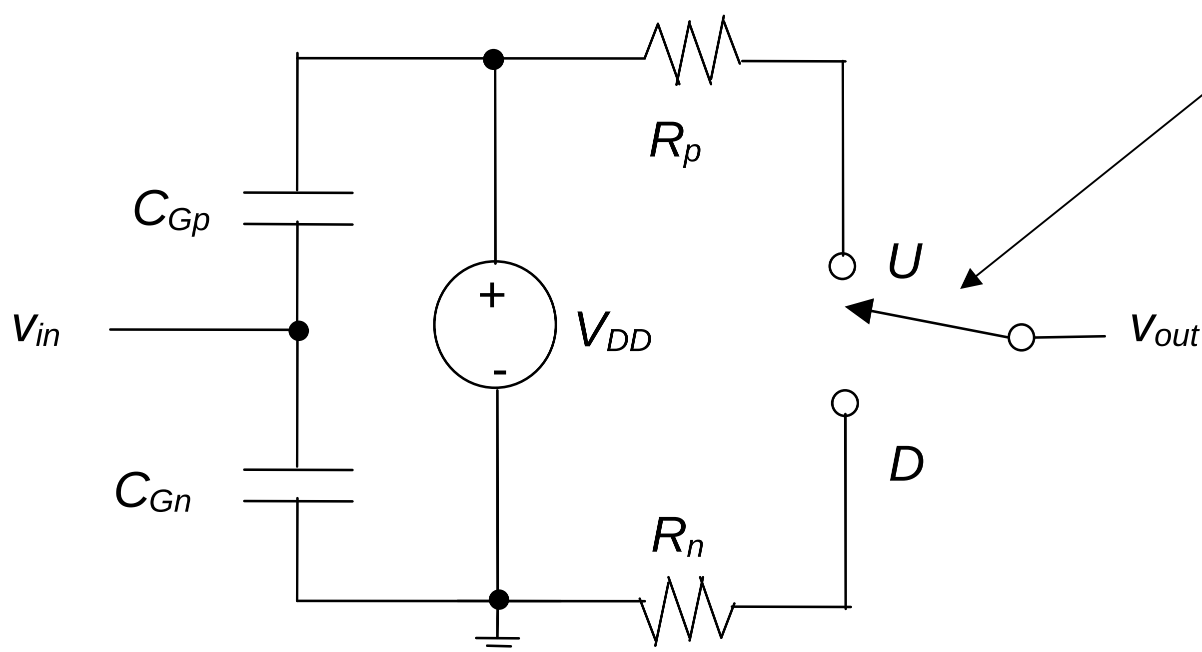
First Order CMOS Inverter Model

The switches are "ganged" (move together) since they have essentially the same trip voltages

NMOS is closed when V_{in} high ; PMOS is open

PMOS is closed when V_{in} low ; NMOS is open

Reduce to a single switch: (Whose position depends on V_{in})

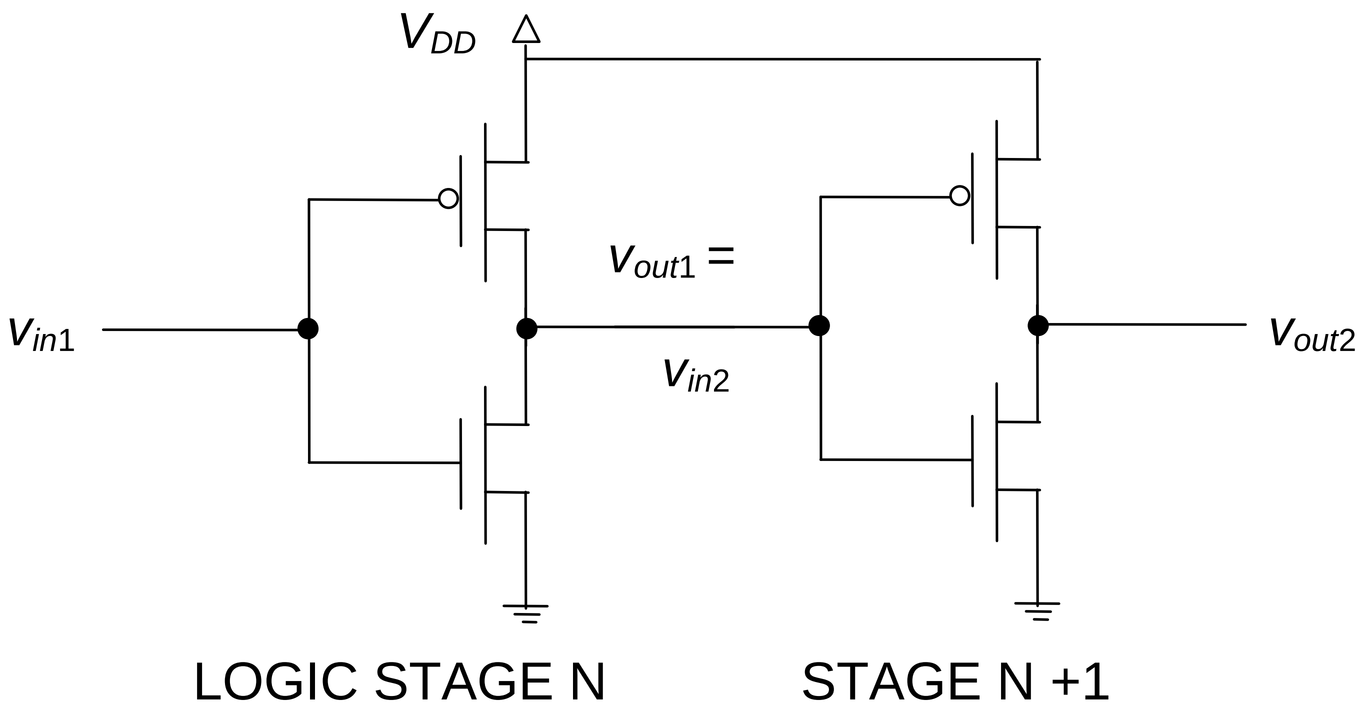


This switch position instantaneously determined by the Gate-to-source voltage (V_{in}).

"Cascaded" CMOS Inverters

What's connected to the v_{out} node? Answer: One or more logic gates, for example another CMOS inverter

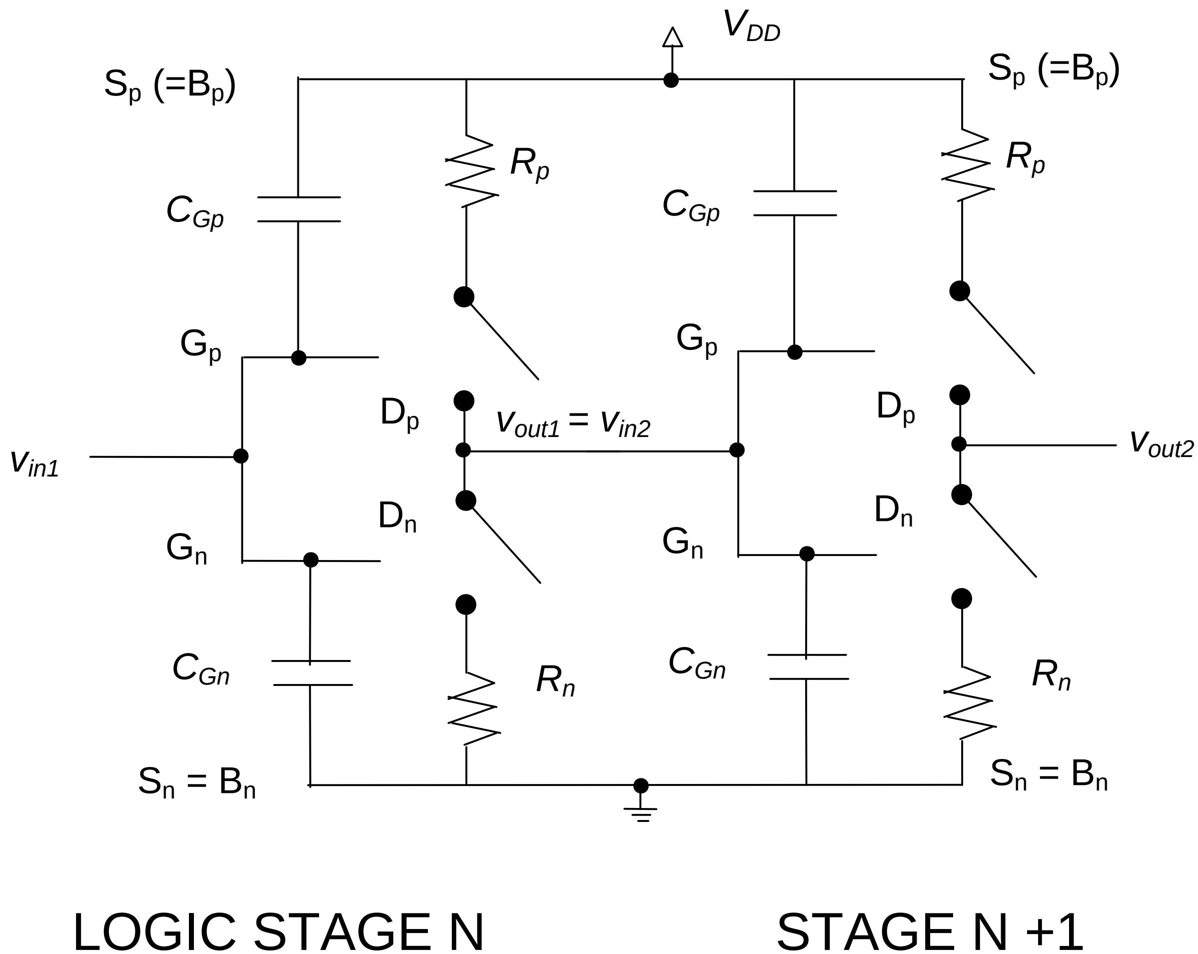
Note that there are no resistors, capacitors, inductors in a CMOS circuit -- there are only NMOS and PMOS transistors.



Cascaded Identical CMOS Inverter Circuit Model

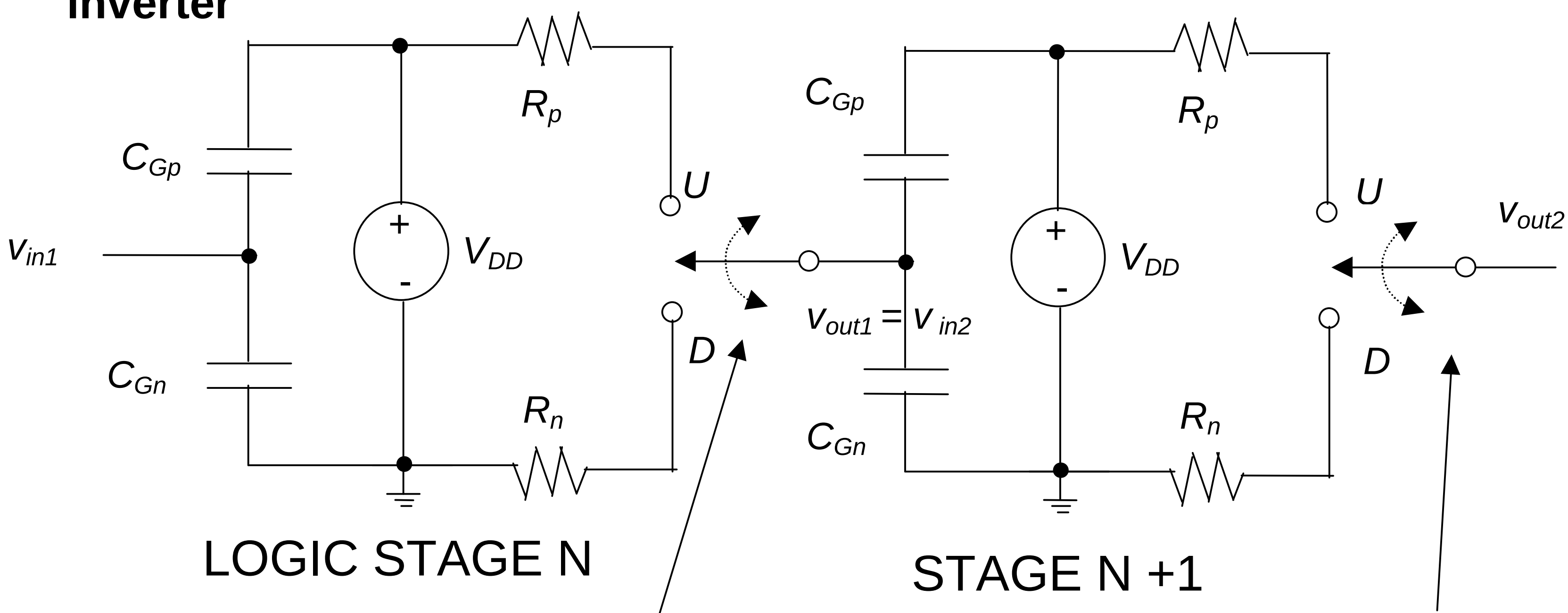
Full switch model showing gate capacitances.

Note that it is the gate capacitance of Stage N +1 combined with the drain resistance of Stage N that slow the gate charging of Stage N +1.



Simpler Representation

NMOS and PMOS transistors have the same logic thresholds, but operate in a complementary fashion → reduce to a single switch per inverter

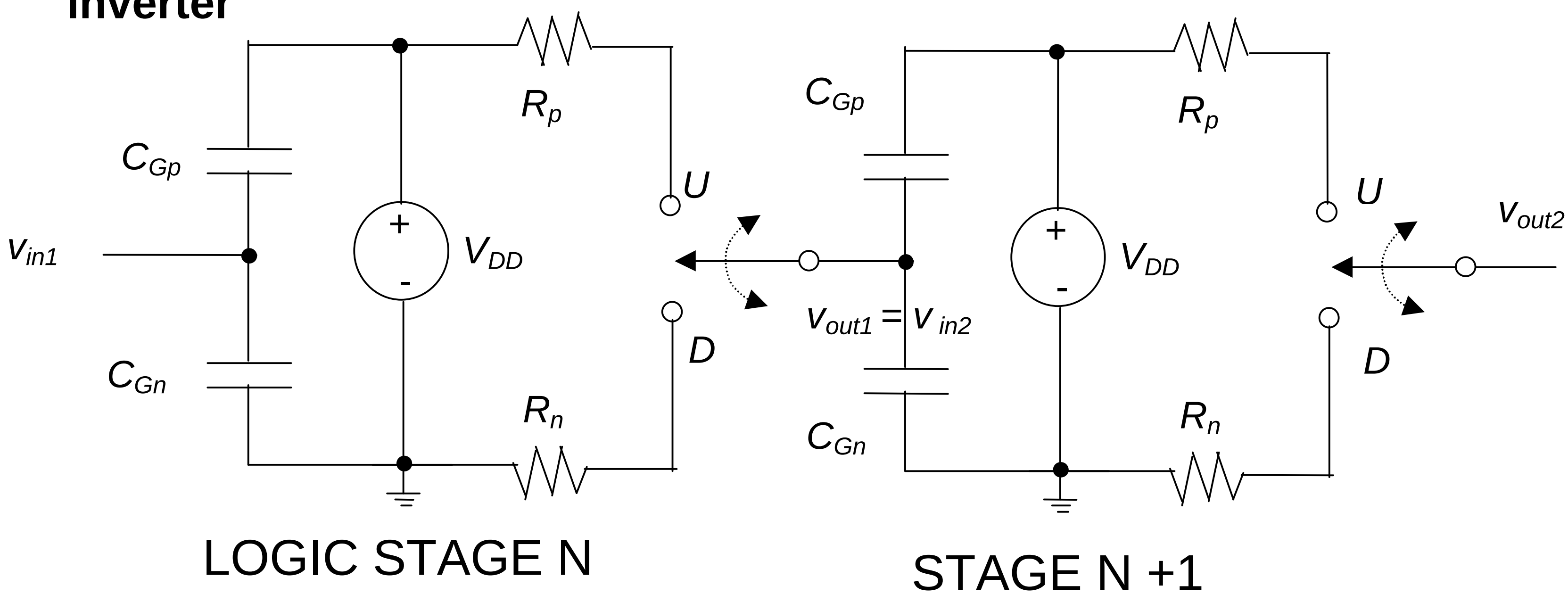


This switch is “up” if V_{in1} is low and “down” if V_{in1} is high.

This switch is “up” if V_{in2} is low and “down” if V_{in2} is high.

Simpler Representation

NMOS and PMOS transistors have the same logic thresholds, but operate in a complementary fashion → reduce to a single switch per inverter

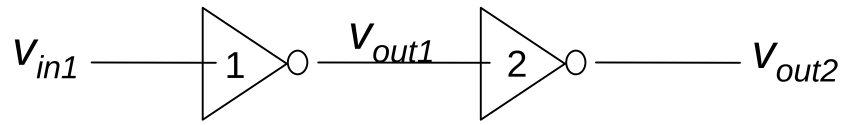


Transitions of interest:

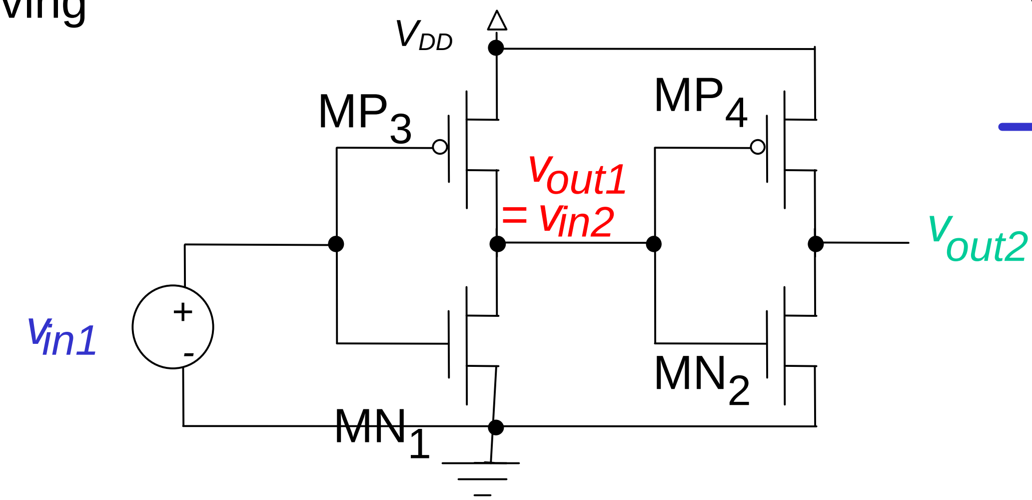
1. v_{in1} goes high : switch for inverter 1 moves to "D" position from previous "U" position (and subsequently output switch goes to "U")

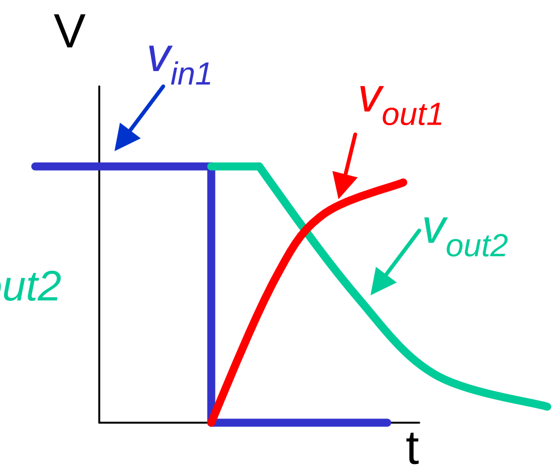
2. v_{in1} goes low : switch for inverter 1 moves to "U" position from previous "D" position (and subsequently output switch goes to "D")

Gate-Delay Analysis -- Identify key Components



Basic case: one inverter driving another





Suppose V_{in1} goes from high to low. ➜ MP_3 turns on and MN_1 turns off.

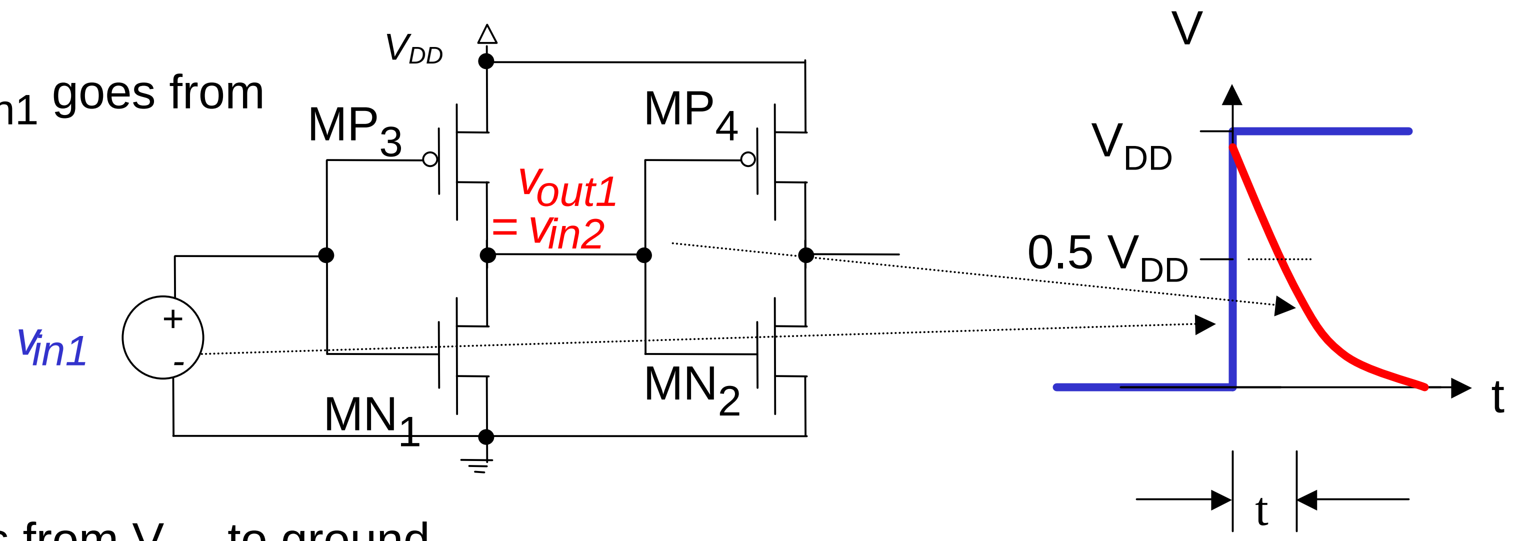
Then V_{out1} goes from low to high (but a little bit later … i.e. delayed).

Of course V_{in2} is the same as V_{out1} .

Thus V_{out2} goes from high to low (delayed even more from the input V_{in1}).

How to define the inverter delay

Suppose V_{in1} goes from low to high.



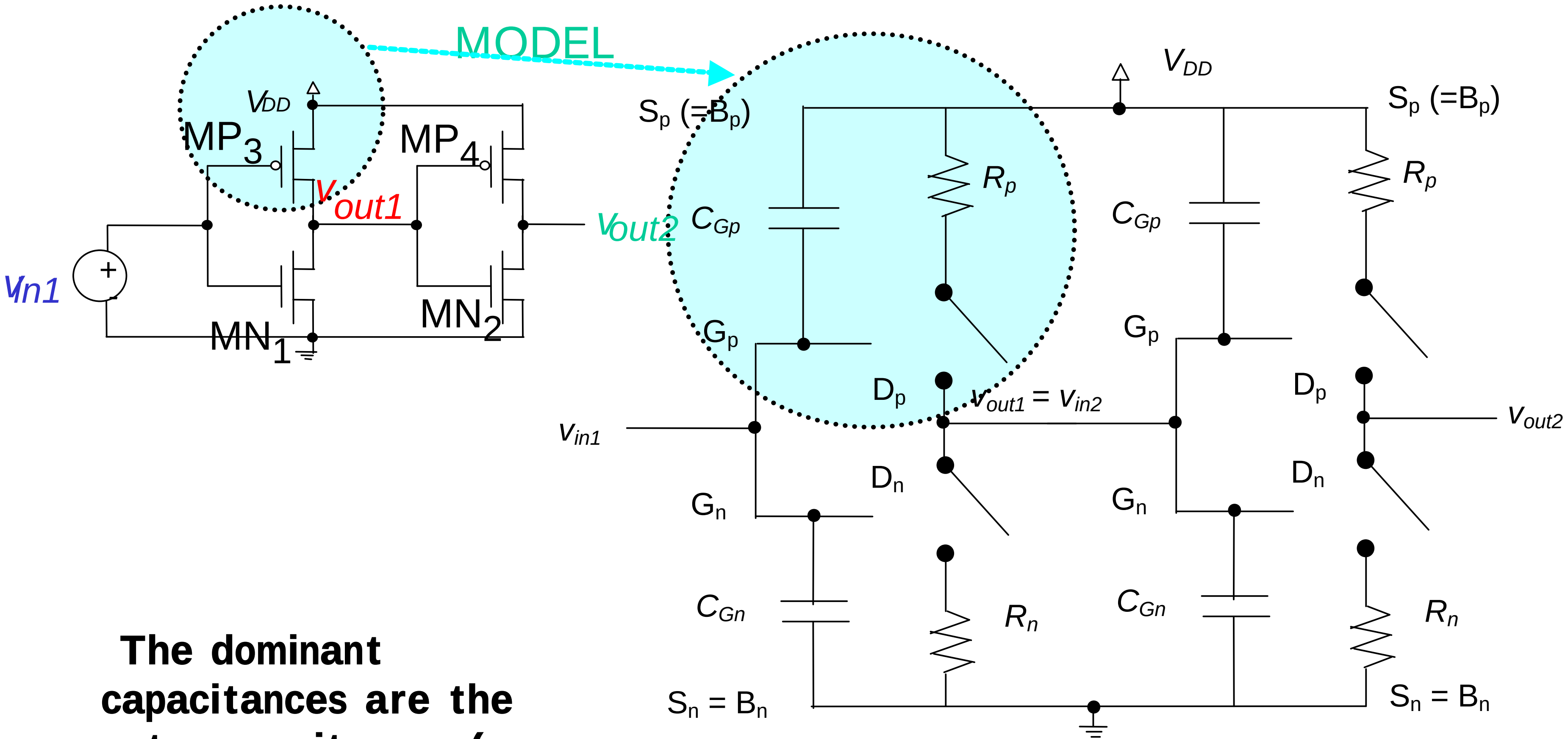
V_{out1} goes from V_{DD} to ground.

We define the inverter stage delay t as the time until V_{out1} reaches V_{DD} /2 .

Because when it reaches this value, the following stage will sense that its input has switched from high to low.

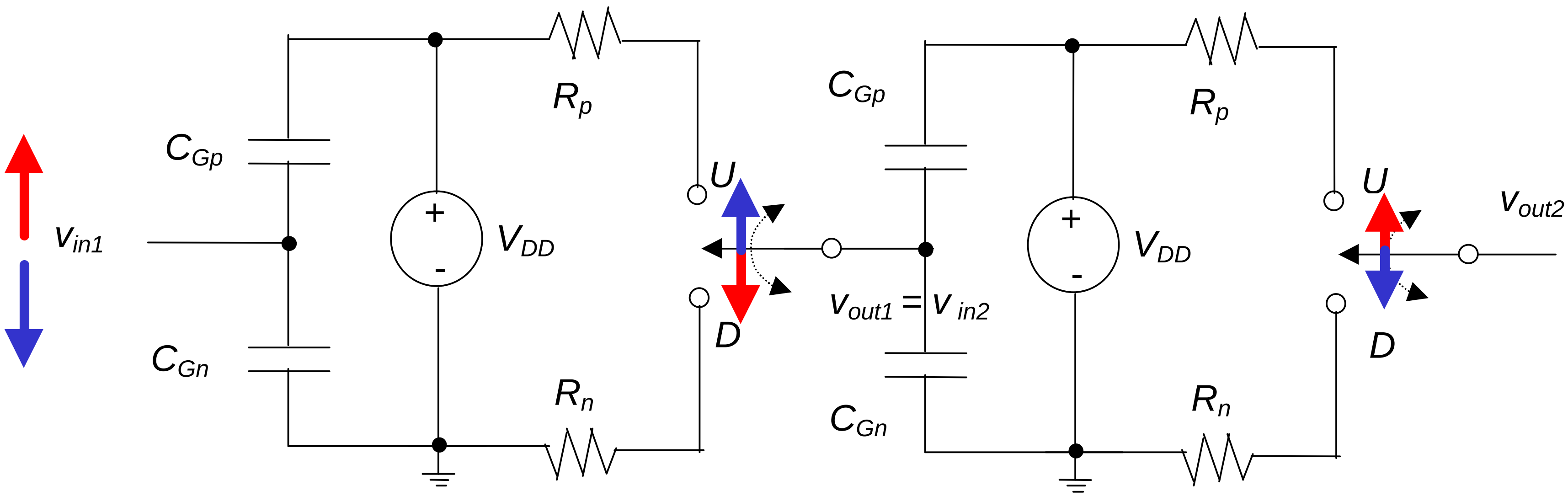
The properly designed stage will have nearly the identical stage delay time for rising input as for falling input. (Design proper ratio of W_p to W_n)

Cascaded Identical CMOS Inverter Circuit Model



The dominant capacitances are the gate capacitances (say 60-90% of total). Hence we omit the others for simplicity here.

Simpler Representation



Transitions of interest:

1. V_{in1} increases above V_{Th} : switch for inverter 1 moves to "D" position from previous "U" position. Of course V_{out2} will follow (switch up).

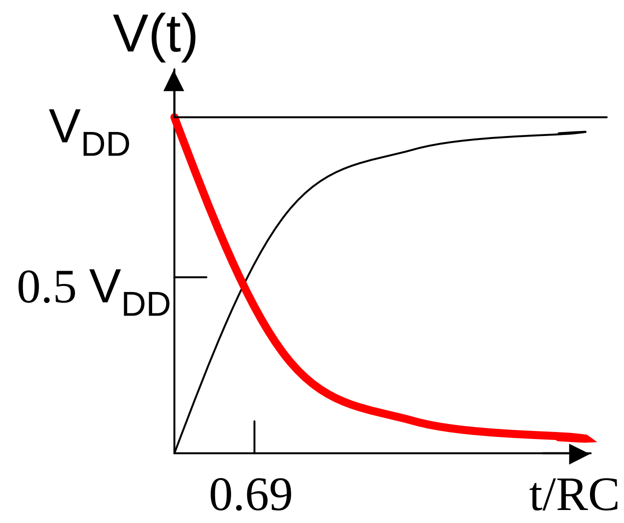
2. V_{in1} decreases below V_{Tl} : switch for inverter 1 moves to "U" position from previous "D" position. Of course V_{out2} will follow (switch down).

Where's the Delay?

Suppose the switch moves instantaneously … what is the origin of gate delay?

Cascaded inverters → input capacitance of the second inverter ("the load") must be charged (or discharged) by current from the first inverter ("the driver") … this takes time! (And there are additional capacitances at this node…)

But we can compute the delay easily . It is just an RC delay. If we define the switching delay as the time for the output voltage to swing halfway to its new steady-state value, we will find the switching delay is 0.69RC.



Remember if $V(t) = V_{DD}\exp(-t/RC)]$
then $V(t) = V_{DD}/2$ at $t = 0.69RC$.

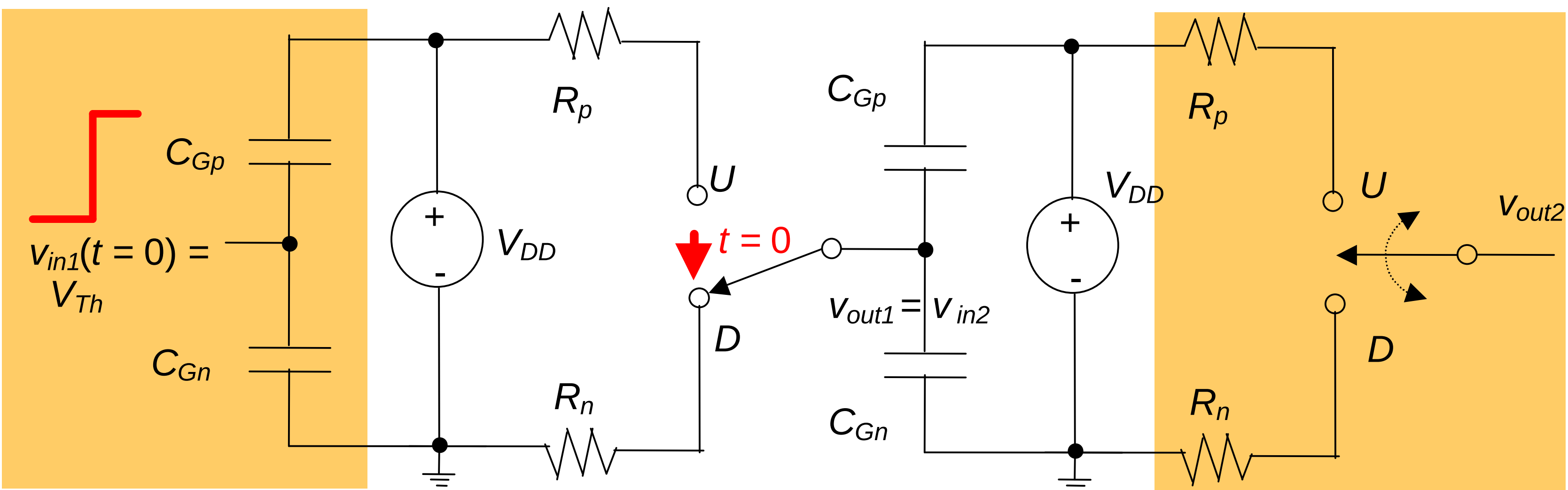
[Because $0.5 = \exp(-0.69)$]

Where's the Delay?

Equivalent circuit for transition 1: note that $v_{out1}(t = 0+) = V_{DD}$

Shaded areas play no role in finding $v_{out1}(t)$.

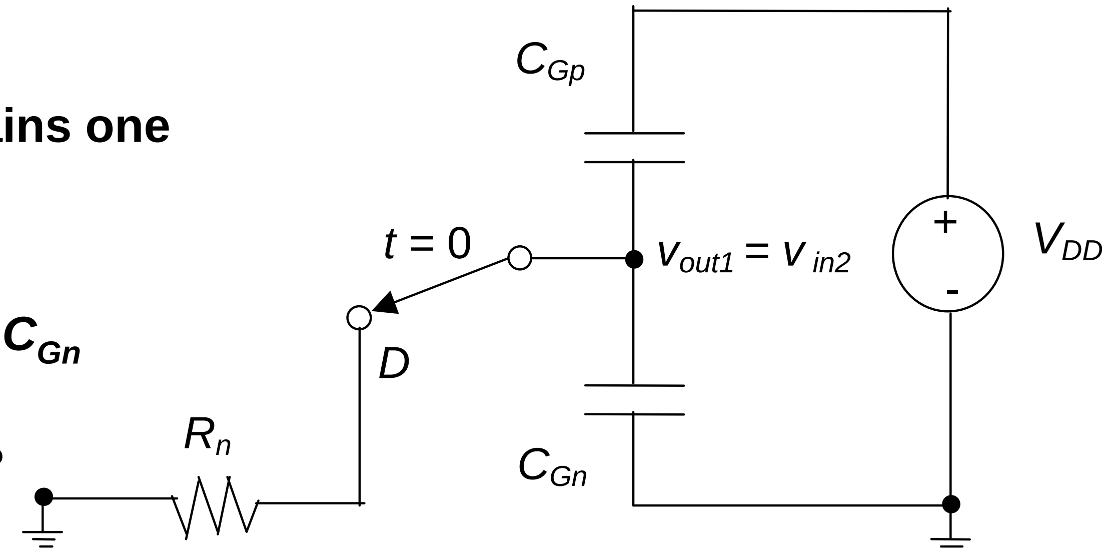
So lets redraw the circuit with essential elements only …… eliminate shaded stuff.



Core Circuit for "Pull-Down" Transition

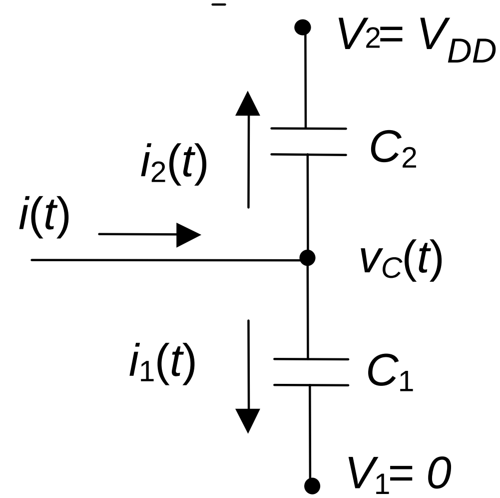
Circuit only contains one resistor and two capacitors

Capacitors C_{Gp} and C_{Gn} … how can they be combined into one?



Capacitors share one node; the other nodes are held at constant voltages.

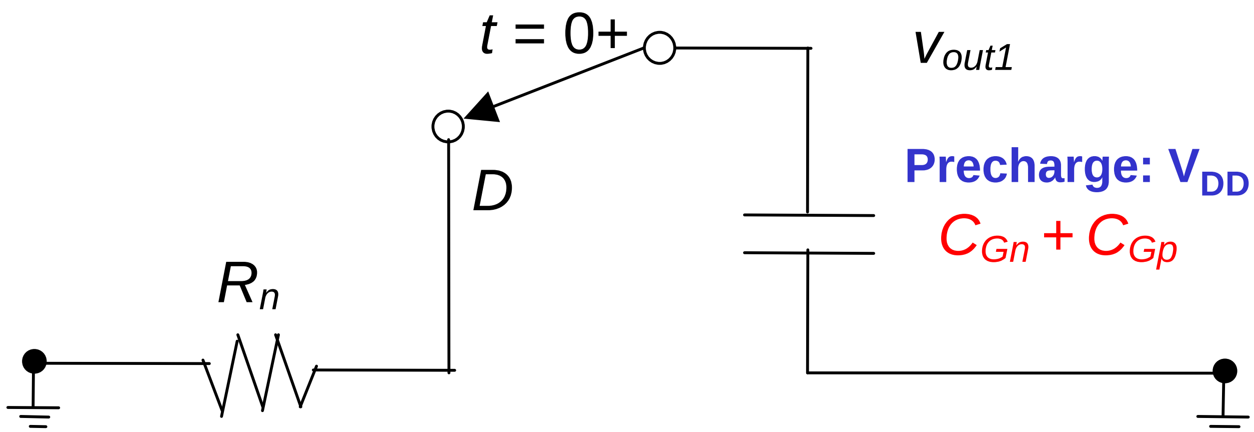
KCL: currents sum at common node, ie node capacitance is SUM (parallel capacitor formula).



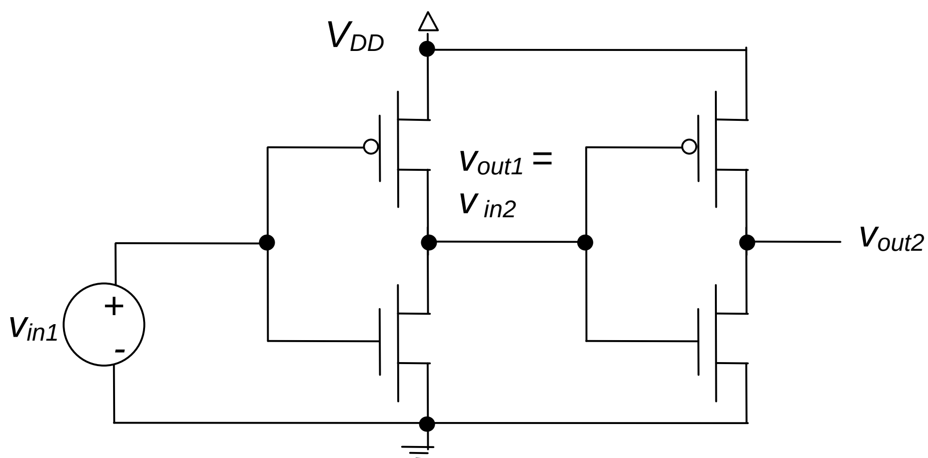
"Virtually Parallel" Capacitors

Pull-Down Equivalent Circuit

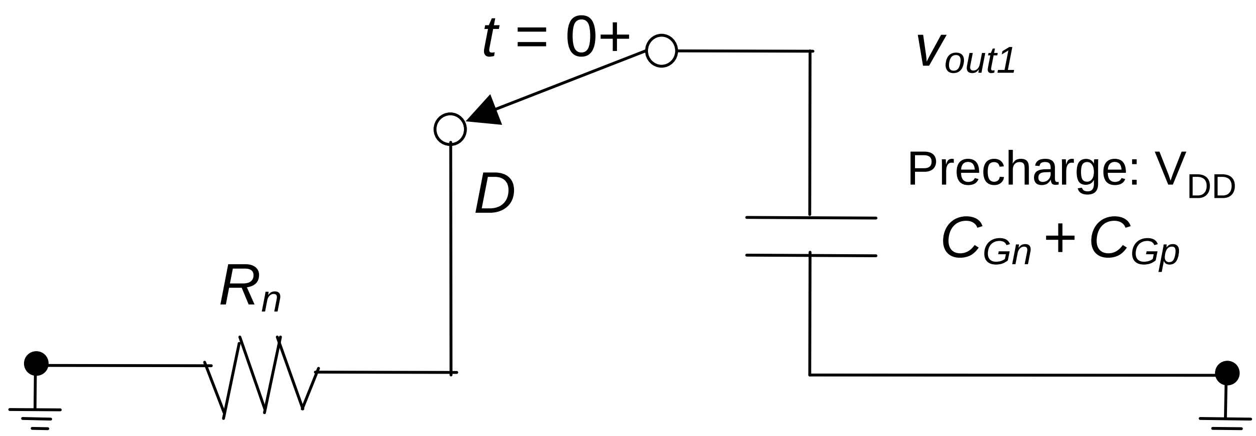
Two capacitors add for finding the charging current → applies to gate capacitances



Before solving lets once more associate circuit above to the actual inverter circuit.



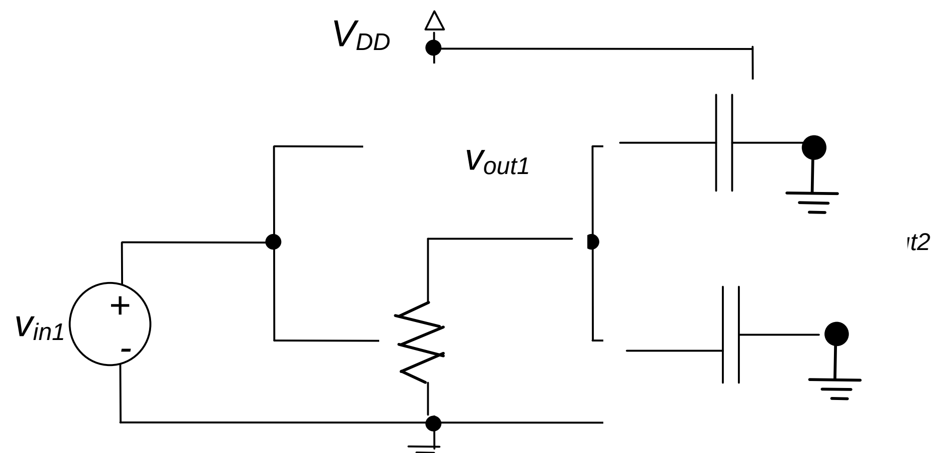
Equivalent circuit vs actual circuit



1) Remove inactive device

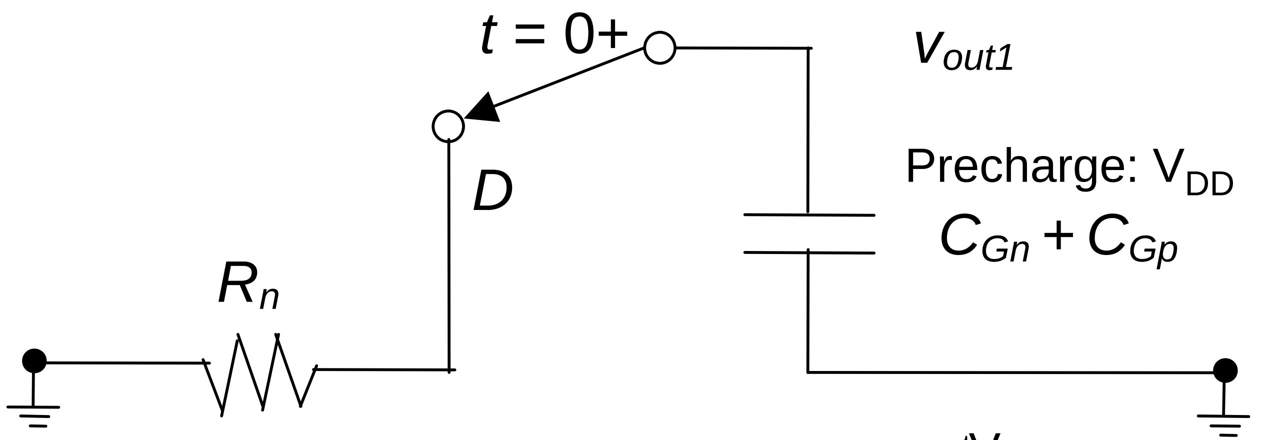
2) Replace load devices by their input equivalents

3) Replace NMOS pull-down by by its output equivalent.



Gate Delay from Pull-Down Equivalent Circuit

Capacitor is precharged to V_{DD} **and discharged to ground through resistance** R_n**.**



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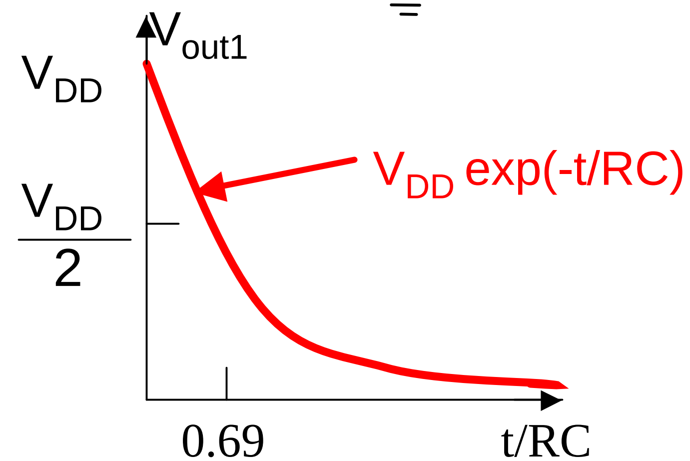
[remember 0.5 = exp(-0.69)]

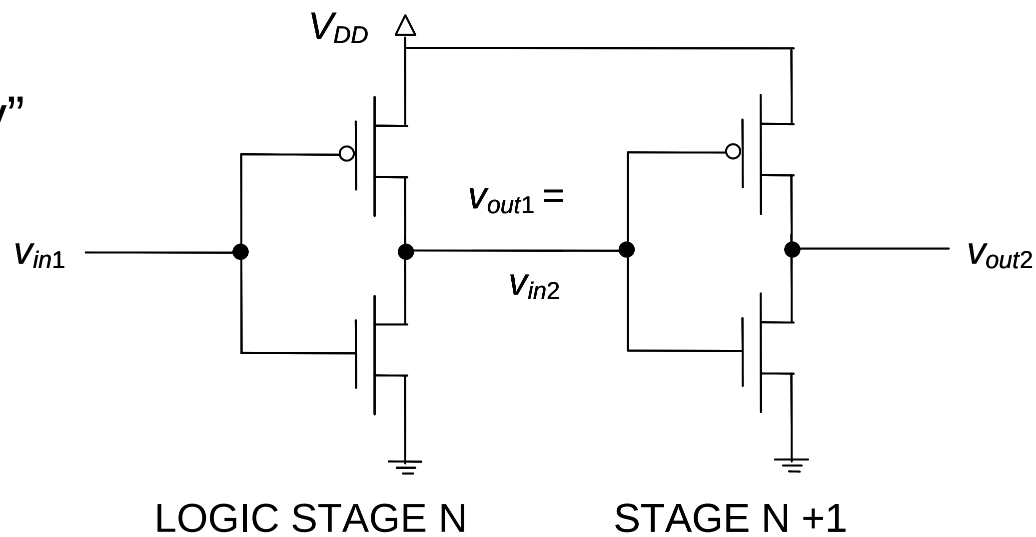


Typical values:

Consider "0.25μm technology"

with a typical NMOS device

0.25 X 1 μm as pulldown



The typical R_{DN} value is 4KΩ

and the typical minimum load value is 5fF.

Thus RC = 20 pS

and the stage delay would be .69 X 20 or 14pS.