

Lecture 26

Last time:

NMOS Transistor

(NMOS = n-channel Metal Oxide Semiconductor Transistor)

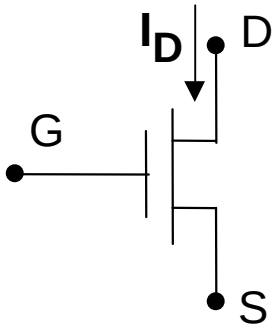
NMOS I-V Characteristics and empirical model (equations)

Today:

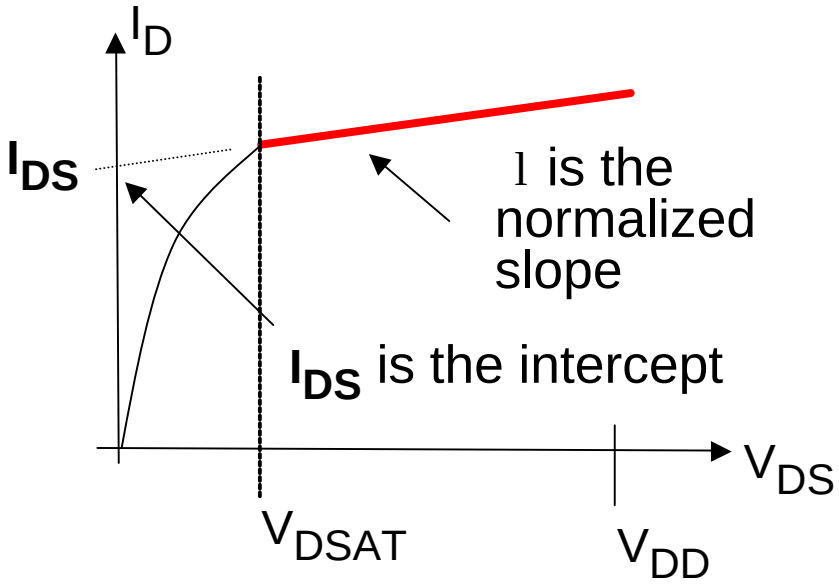
- **NMOS Switch Model**
- **PMOS transistor and Switch Model**
- **CMOS!**

NMOS Review

The variation of I_D with V_{DS} in the saturation region is given by:



$I_D = I_{DS} \times (1 + \lambda V_{DS})$ in which I_{DS} is proportional to the channel width W and depends on the Gate Voltage above threshold. If $V_{GS} < V_t$ then $I_D = 0$.



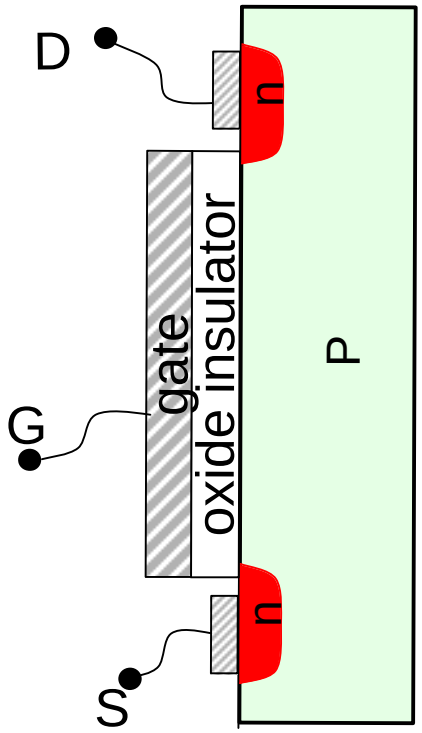
Thus for our hand calculations we need only to have the following MOS properties specified:

1) Saturation Current I_{DS}

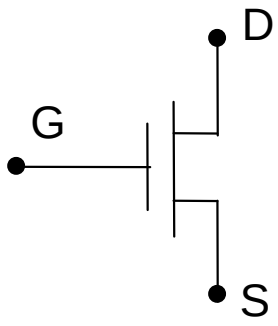
2) The slope λ. This is the fractional increase of current for one volt increase in V_{DS}.

3) We may not need to know V_{DSAT} because we will be typically interested in the current in the range $V_{DS} > V_{DD}/2$.

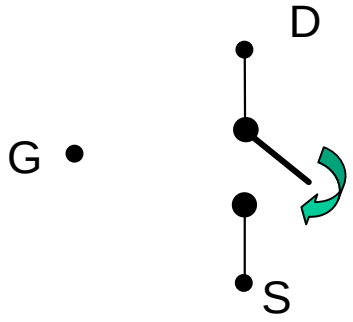
MOS Transistor "Switch Model"



Physical NMOS Device



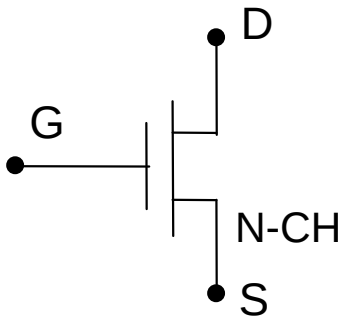
Circuit Symbol for the MOS Device



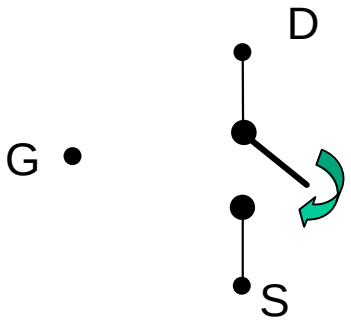
Possible Electrical Model

- **No current flows through the gate terminal of a MOS Device**
- **But the Gate voltage controls the resistance from drain to source**

NMOS Transistor "Switch Model"



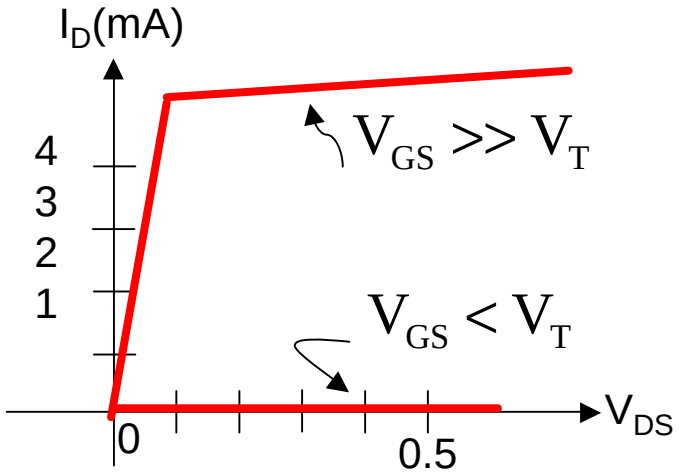
Circuit Symbol for the NMOS Device



Possible Electrical Model

THE THRESHOLD CONCEPT:

- If V_{GS} < a threshold voltage, V_T, Switch is open
- If V_{GS} >> V_T, Switch is closed



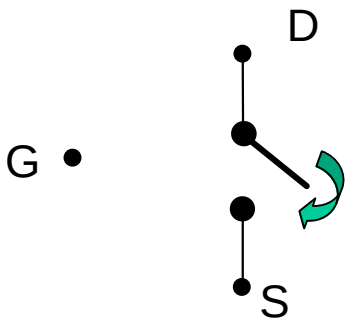
But I_D vs V_{DS} is too complex to be represented by open/short

NMOS Model Refinement

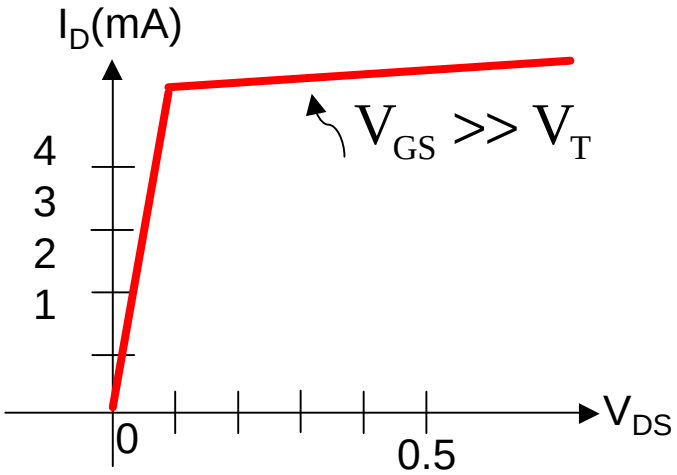
Closed NMOS transistor is not a perfect conductor

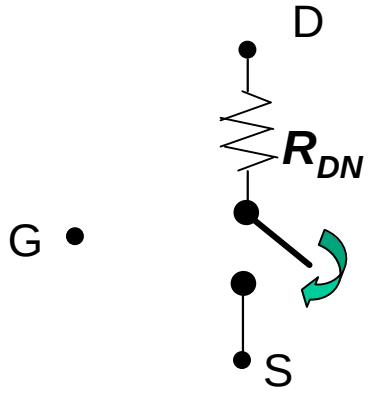
→ add an equivalent resistor R_{DN} that reflects this phenomenon

Note: R_{DN} is NOT the simple source drain resistance near the origin.



Possible Electrical Model





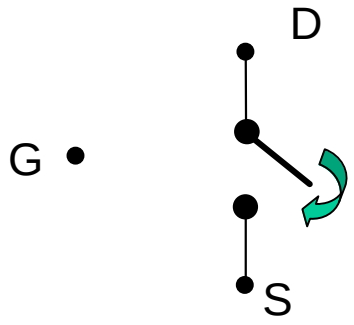
Improved Electrical Model

R_{DN} depends on 1) Gate voltage , and 2) Device geometry ***Why?***

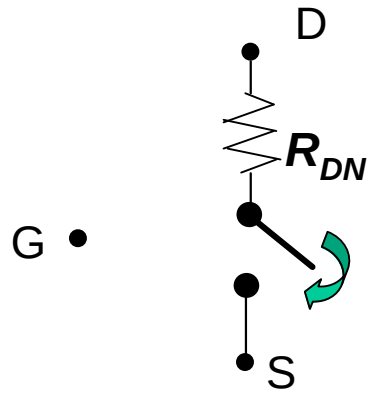
We will use $v_{GS} = 0$ for open switch and $v_{GS} = v_{DD}$ for closed switch. Thus there is only one "on" gate voltage.

R_{DN} will be inversely proportional to the gate width W.

NMOS Model



Simplified Electrical Model

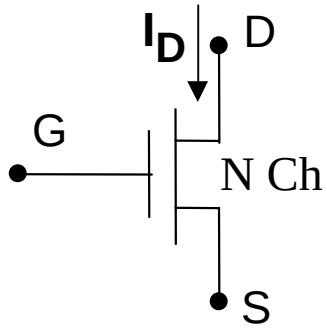


Improved Electrical Model

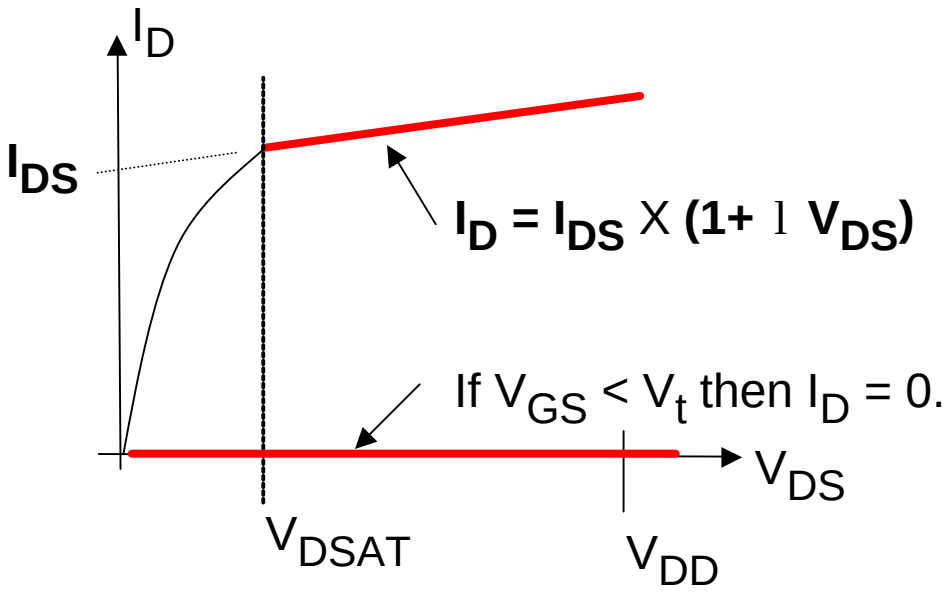
Note: R_{DN} is NOT the simple (low V_{DS}) source drain resistance

- If $V_{GS} = 0$ we have open switch (or $R_{DN} = 8$).
- If $V_{GS} = V_{DD}$ we have closed switch. R_{DN} is only an effective resistor value. We need to choose the value of R_{DN} that gives the correct answer for timing calculations.
- Before finding R_{DN} we need to consider the actual device structure. (next lecture)

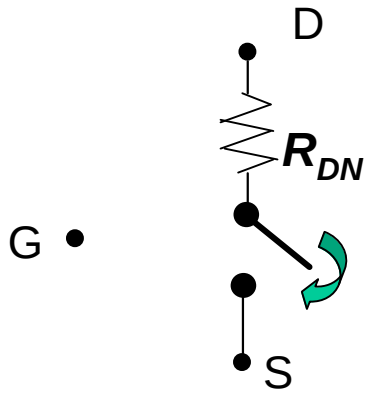
NMOS Summary



The circuit symbol

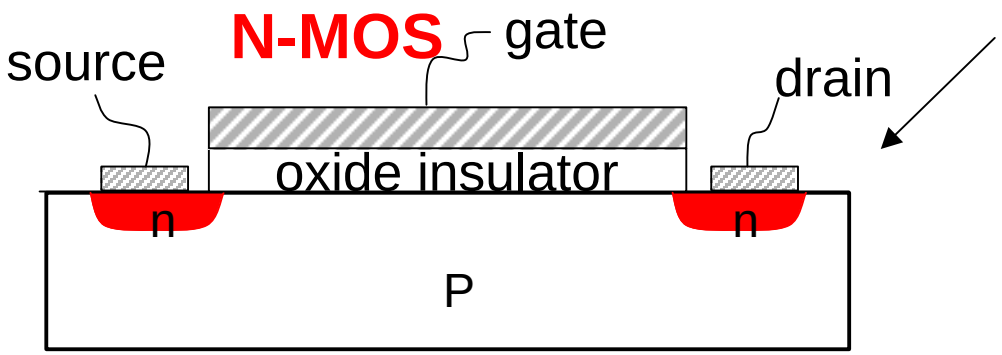


In NMOS, typically all values are positive. For example, $V_t = 0.5$ V, $\lambda = 0.05$, $V_{DD} = 2.5$V, $V_{DSAT} = 1$V, $I_{DS} = 0.1$mA at $V_{GS} = V_{DD}$.



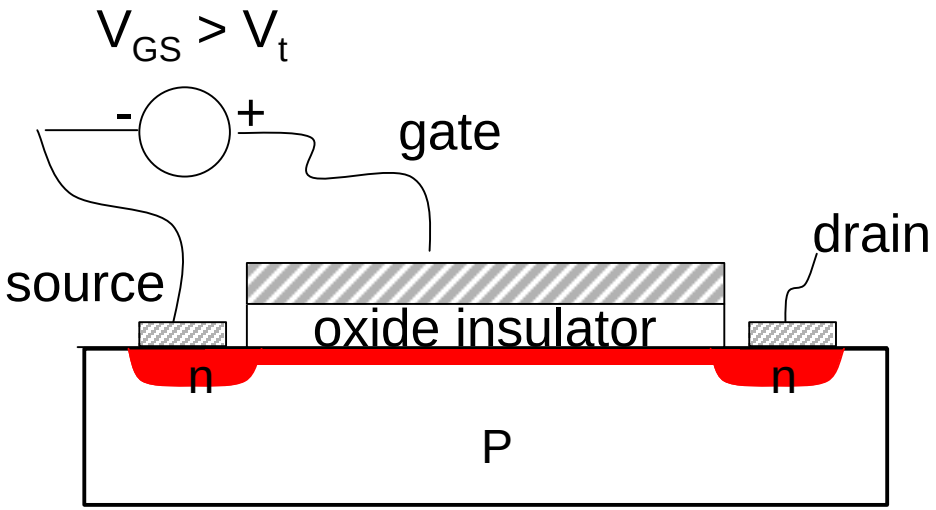
Electrical Model

NMOS =device which carrier current using electrons but on the surface of a p-type substrate



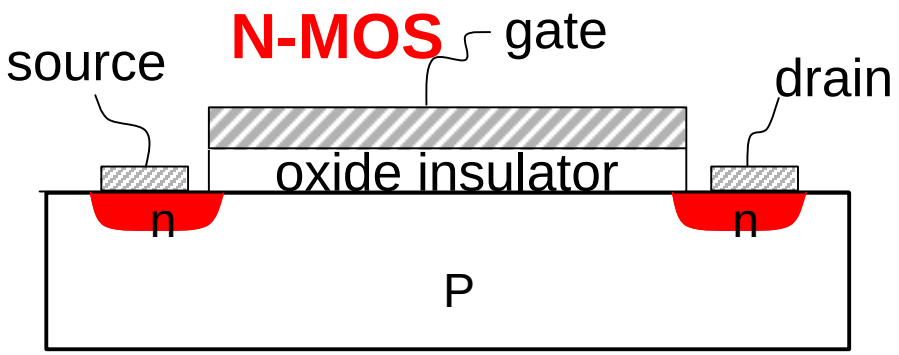
In this device the gate controls electron flow from source to drain.

(in the absence of gate voltage, current is blocked)



If we increase gate voltage to a value greater than V_t then a conducting channel forms between source and drain. ("Closed switch")

CMOS = Complementary MOS (PMOS is a second Flavor)



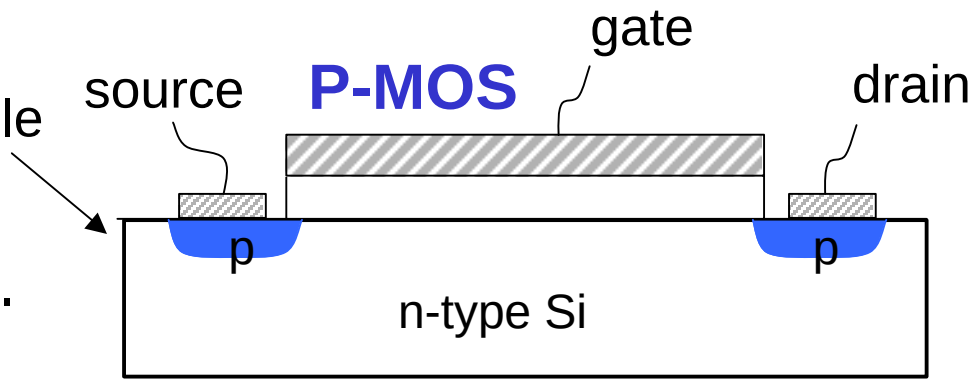
In this device the gate controls electron flow from source to drain.

It is made in p-type silicon.

The NEW FLAVOR! **P-MOS**

In this device the gate controls hole flow from source to drain.

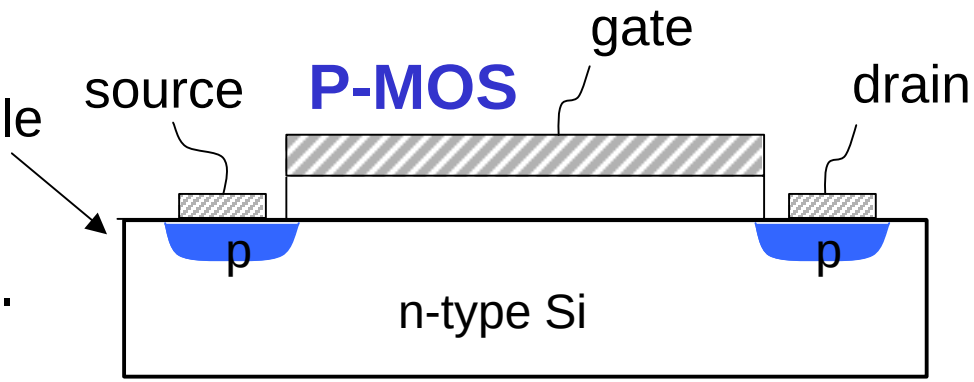
It is made in n-type silicon.

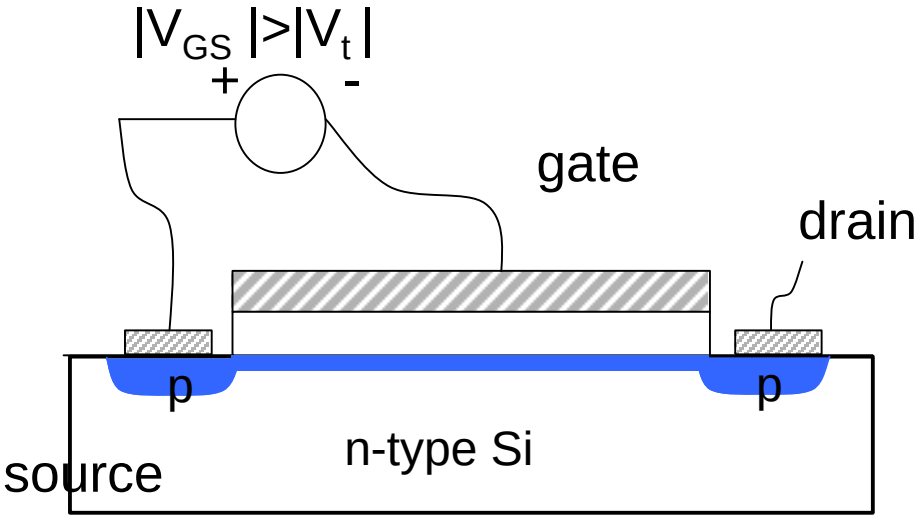


PMOS

In this device the gate controls hole flow from source to drain.

It is made in n-type silicon.





What if we apply a big negative voltage on the gate?

If $|V_{GS}|>|V_t|$ (both negative)

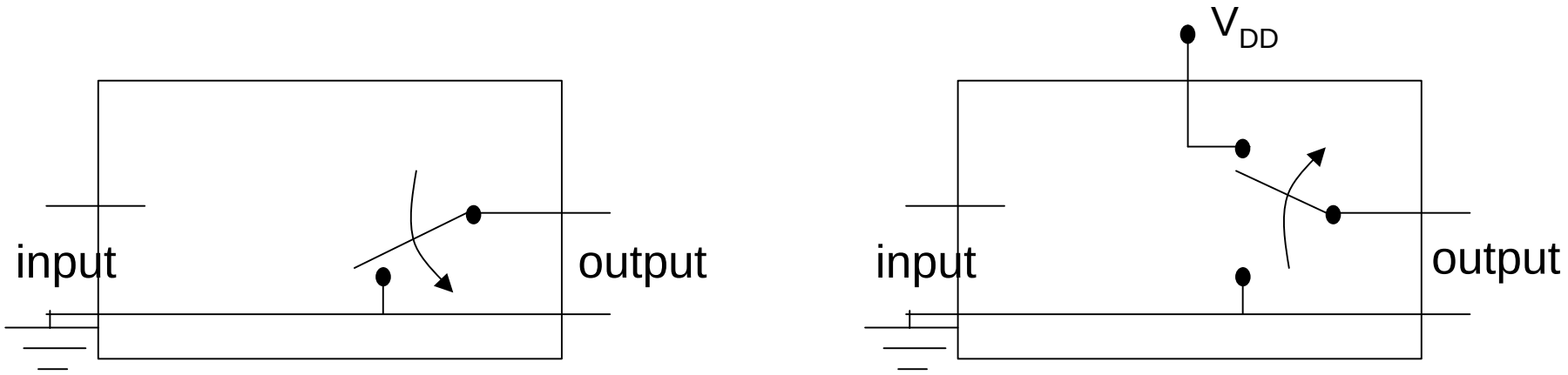
then we induce a + charge on the surface (holes)

Why do we want PMOS?

We already have the ideal switch to connect any node to ground.

An NMOS transistor with gate held high has a very low resistance and essentially switches a node to ground (logic low).

We also need a switch to switch nodes to whatever voltage is chosen as logic high (typically V_{DD}).

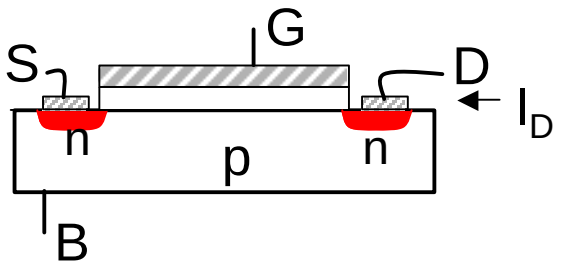


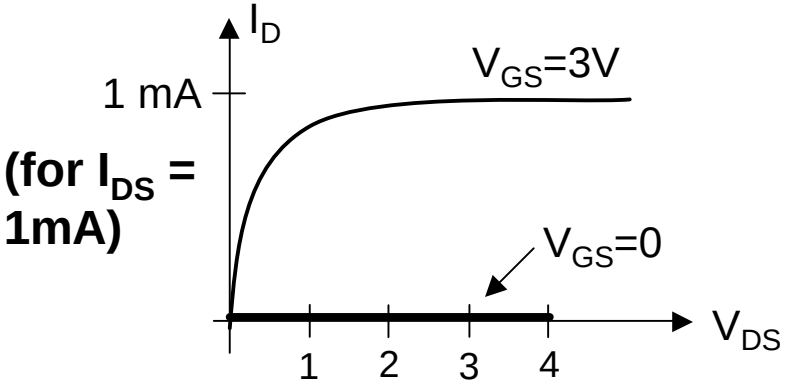
- **A PMOS transistor is just the ticket. It is precisely as ideal a switch for connections to high as NMOS transistors are for connections to low.**
- **What's cool is that there is little more to learn about PMOS. These devices are essentially the same as NMOS except *all signs on V and I are reversed.***

NMOS and PMOS Compared

NMOS

"Body"	–	p-type
Source	–	n-type
Drain	–	n-type
V_{GS}	–	positive
V_T	–	positive
V_{DS}	–	positive
I_D	–	positive (into drain)

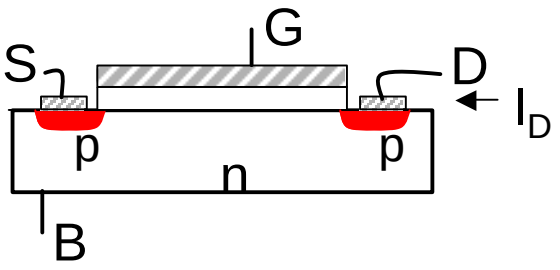


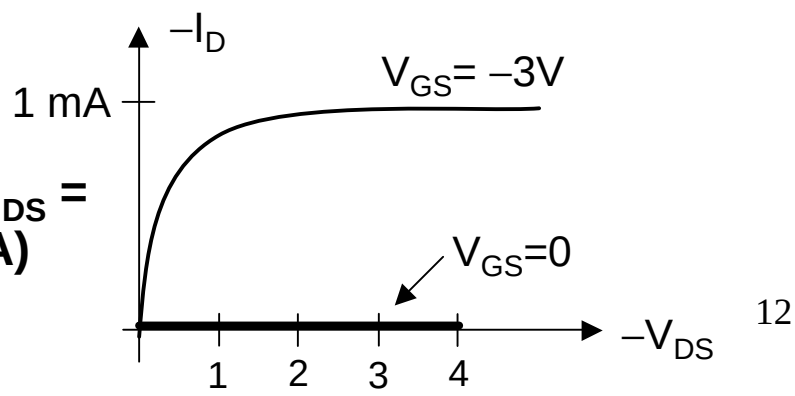


(for I_{DS} = 1mA)

PMOS

"Body"	–	n-type
Source	–	p-type
Drain	–	p-type
V_{GS}	–	negative
V_T	–	negative
V_{DS}	–	negative
I_D	–	negative (into drain)

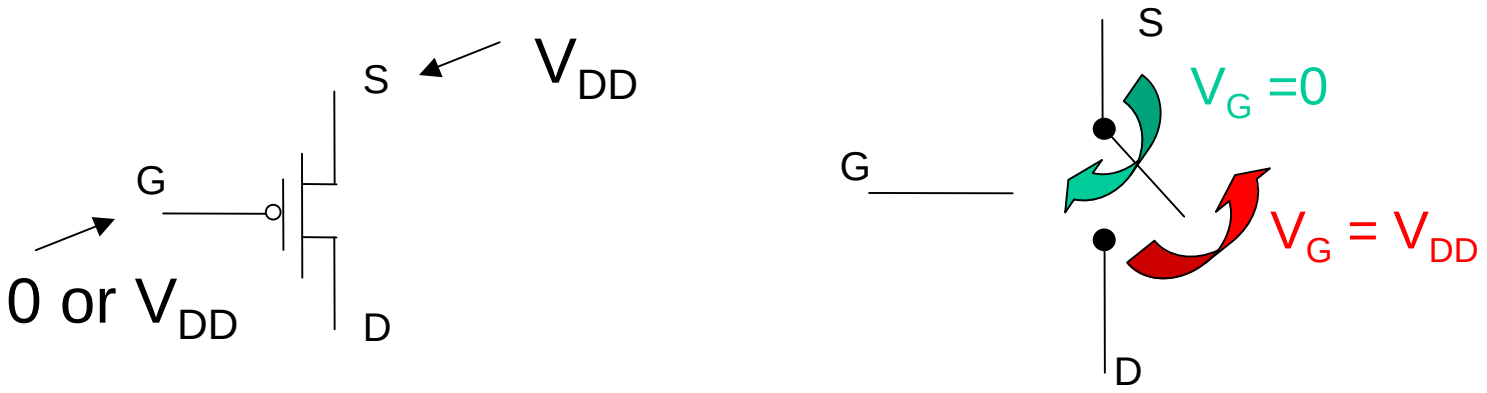




(for I_{DS} = -1mA)

PMOS Transistor Switch Model

"Complementary" operation compared to NMOS



Switching thresholds for PMOS for "default" digital circuit connection

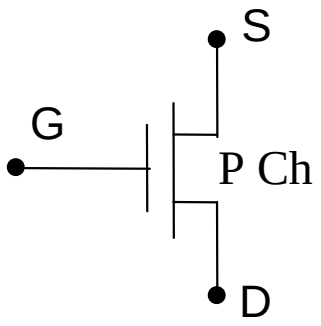
Connect S to VDD (The function of the device is a "pull up")

Switch is *closed:* Drain (D) is shorted to Source (S) when V_G =0

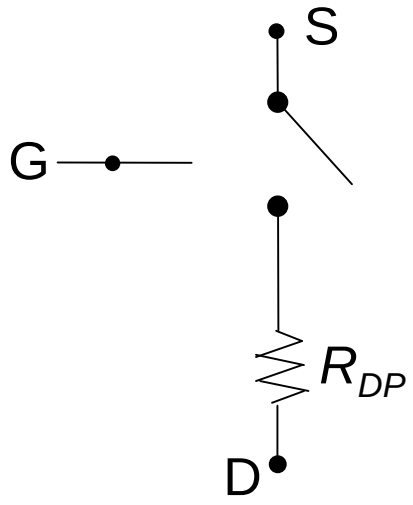
Switch is *open :* Drain (D) is disconnected from Source (S) when $V_G = V_{DD}$

PMOS Model Refinement

PMOS transistor has an equivalent resistance R_{DP} when closed



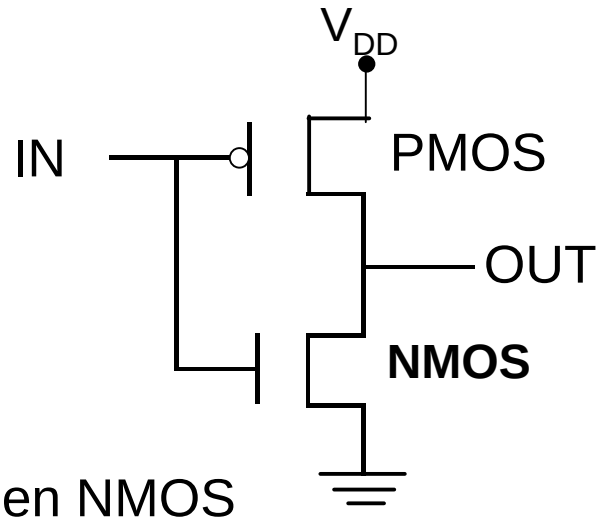
The circuit symbol



The Switch model

CMOS - WHY DO CMOS ??

Basic Circuit: Two switches. One to ground, one to V_{DD}.

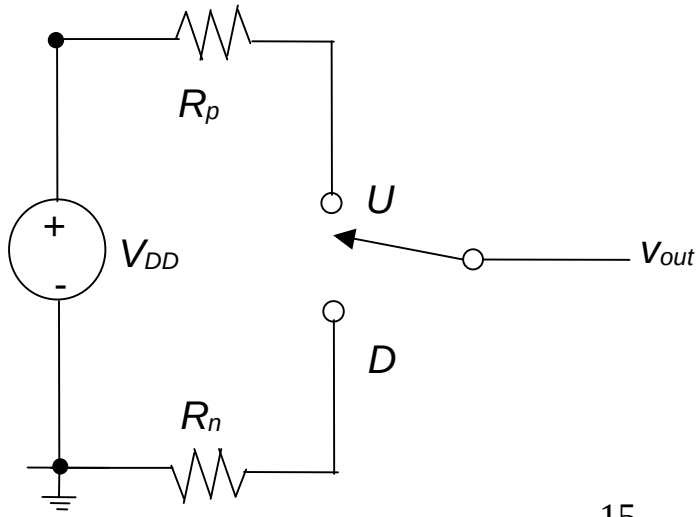


Essential Idea:

Input High (e.g. V_{DD}): Then NMOS is a closed switch to ground and PMOS is an open switch.

Input Low (e.g. 0V): Then NMOS is an open switch and PMOS is a closed switch to V_{DD}.

Clearly the output is an nice logical inversion of the input. INVERTER.



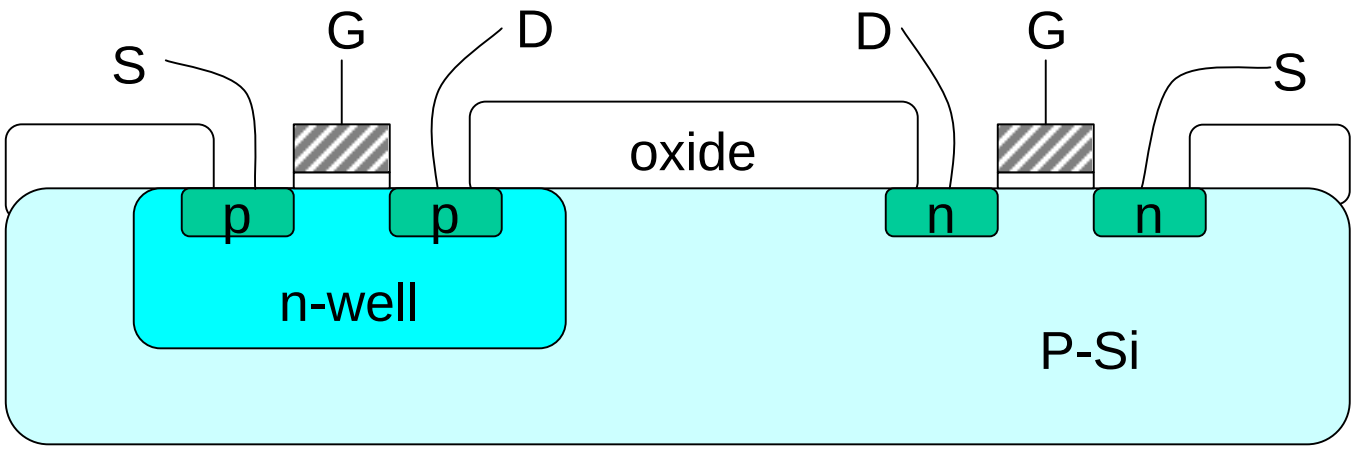
CMOS

Challenge: build both NMOS and PMOS on a single silicon chip

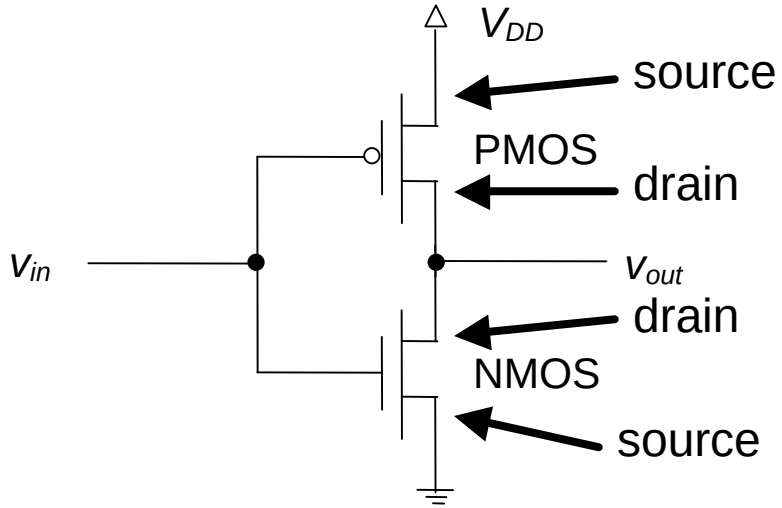
NMOS needs a p-type substrate

PMOS needs an n-type substrate

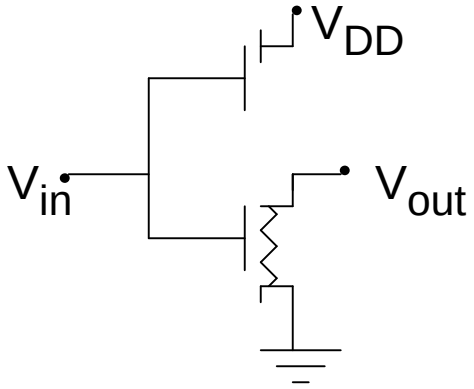
Requires extra process steps



THE BASIC STATIC CMOS INVERTER

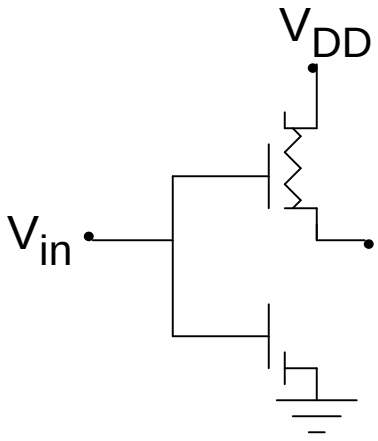


For V_{in} > 1.5V NMOS on , PMOS off



V_{out} **= 0**

For V_{in} < 1V NMOS off , PMOS on



V_{out} **=** V_{DD}

Example for Discussion:

NMOS: V_{Tn} = 1V

PMOS: V_{Tp} = -1V

Let V_{DD} = 2.5V