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Lecture 20

LECT 19 Review

Gate delay in logic circuits

Today: Two Topics

1) Simple controlled switch model of logic

2) Capacitor charging and energy per logic cycle

Review of Energy in Switching

Efficiency

Dynamic Power

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How can we build inverters, Nand gates, etc. ?

We need some sort of controlled switch: that is a device in which a switch opens or closes in response to an input voltage (a control voltage). If we have a controlled switch it is an easy matter to build inverters, Nand gates, etc.

For example an electromagnetic *relay* has a coil producing a magnetic field causing some contacts to “snap shut” when a voltage is applied to the coil.

Lets imagine a simple controlled switch, but include in it some resistance (all real devices have non-zero resistance).

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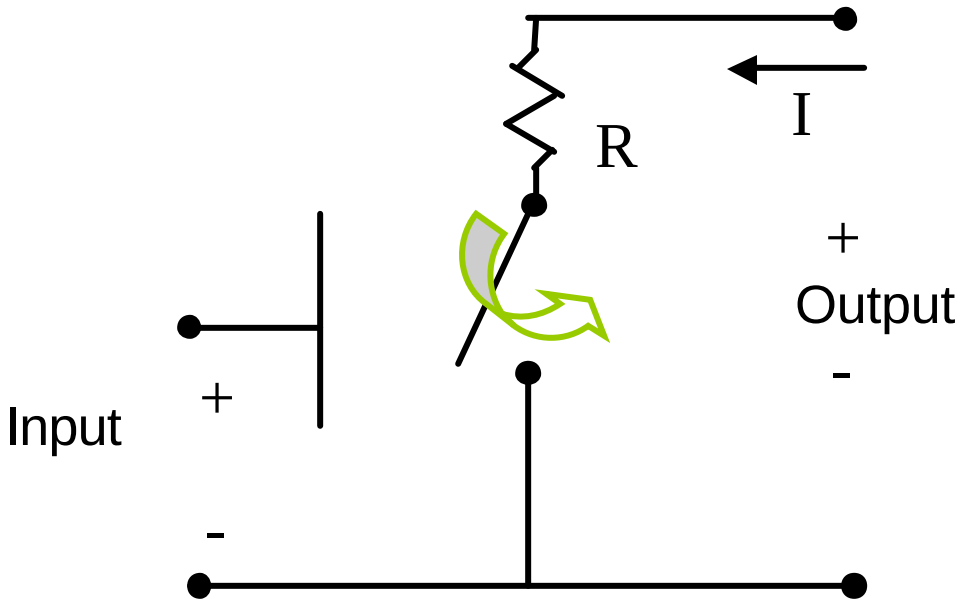
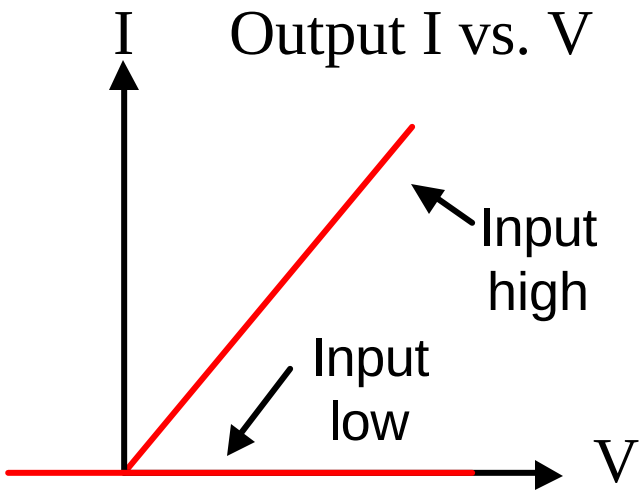
Controlled Switch Model





The basic idea: We need a switch which is controlled by an input voltage. For example: Input V = 0 means the switch is open, whereas an input voltage of 2V means that the switch is closed

(We will call this a “Type N controlled switch”)

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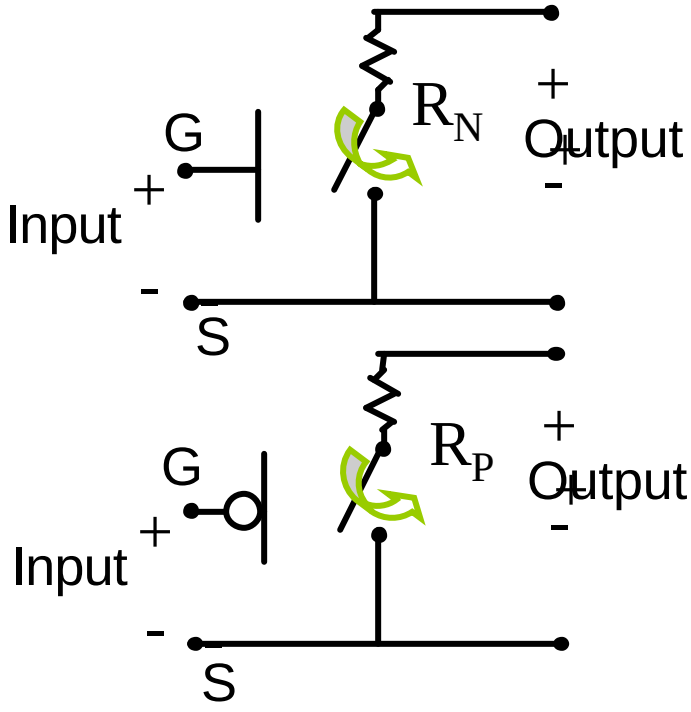
Controlled Switch Model



Type N controlled switch" means switch is closed if input is high. ($V_G > V_S$)

Type P controlled switch" means switch is closed if input is low. ($V_G < V_S$)

Now lets combine these switches to make an inverter.

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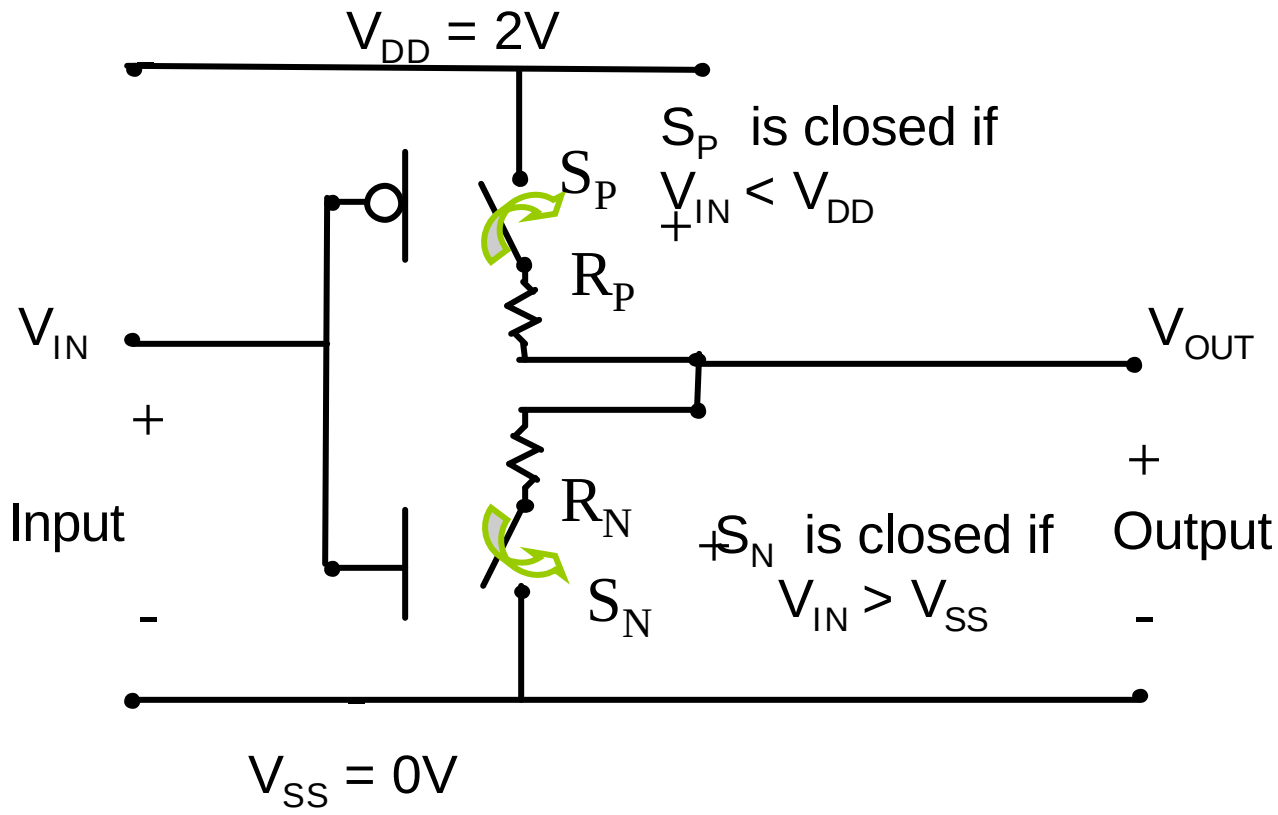
Controlled Switch Model of Inverter



So if V_{IN} is 2V then S_N is closed and S_P is open. Hence V_{OUT} is zero.

But if V_{IN} is 0V then S_P is closed and S_N is open. Hence V_{OUT} is 2V.

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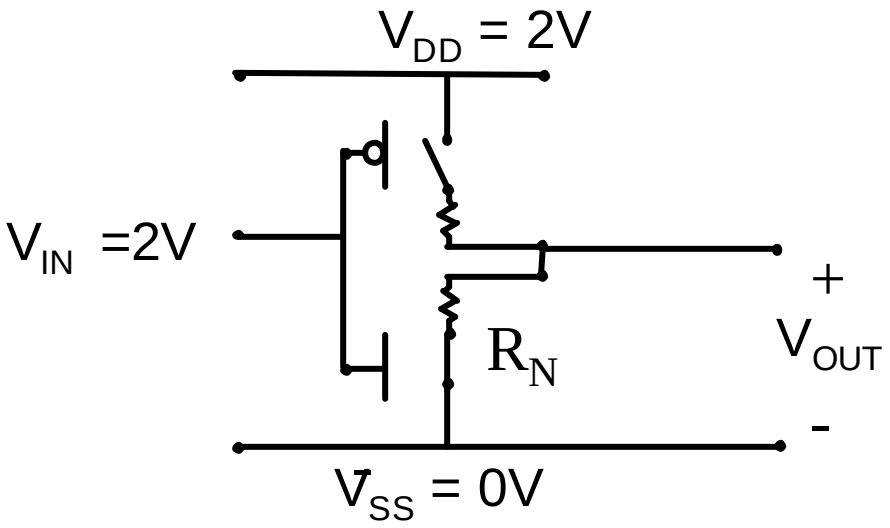
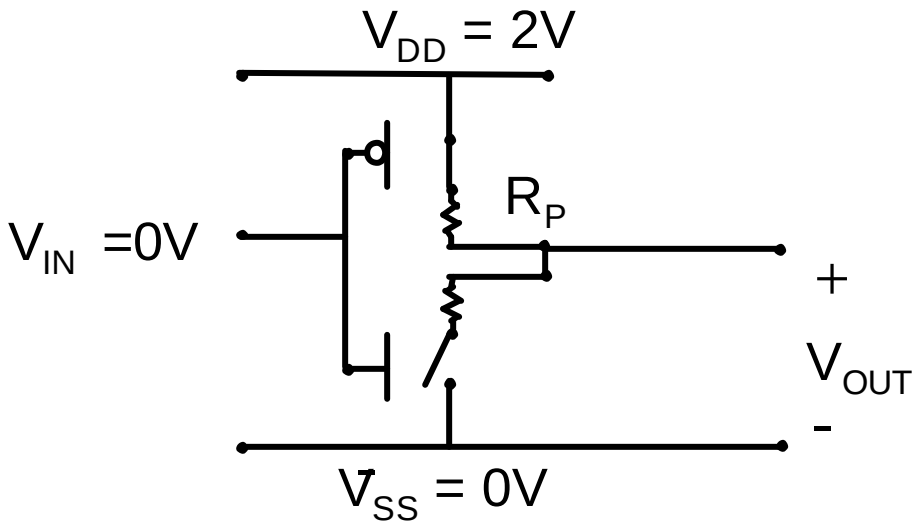
Controlled Switch Model of Inverter



IF V_{IN} is 2V then S_N is closed and S_P is open. Hence V_{OUT} is zero (but driven through resistance R_N).



But if V_{IN} is 0V then S_P is closed and S_N is open. Hence V_{OUT} is 2V (but driven through resistance R_P).

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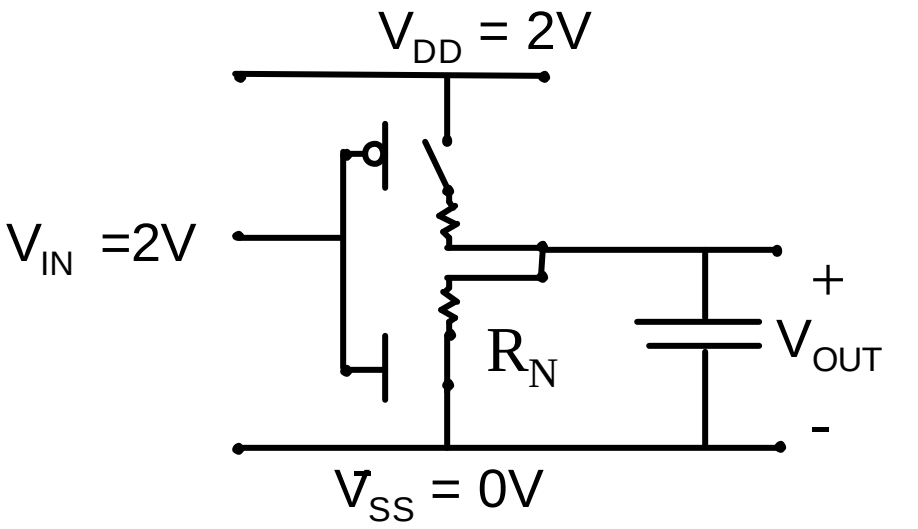
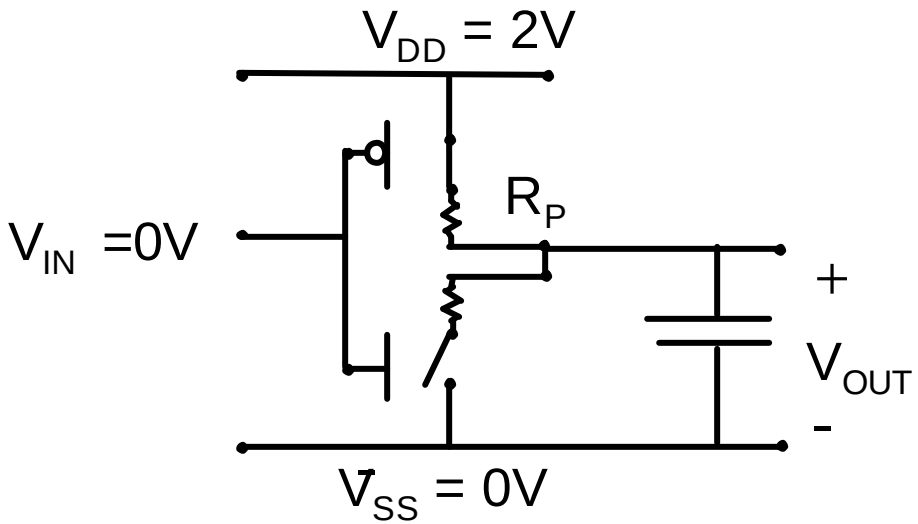
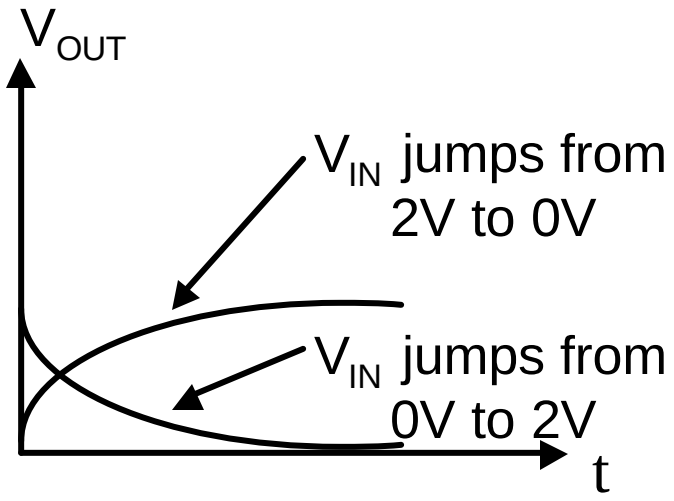
Controlled Switch Model of Inverter





IF there is a capacitance at the output node (there always is) then V_{OUT} responds to a change in V_{IN} with our usual exponential form.



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Controlled Switch Model of Inverter

We will expand on this model in coming weeks.

The controlled switches will of course be MOS transistors.

The resistance will be the effective output resistance of the MOS devices.

The capacitance will be the input capacitance of the MOS devices.

But now lets briefly review the energy used in charging and discharging capacitances so we can start to estimate chip power.

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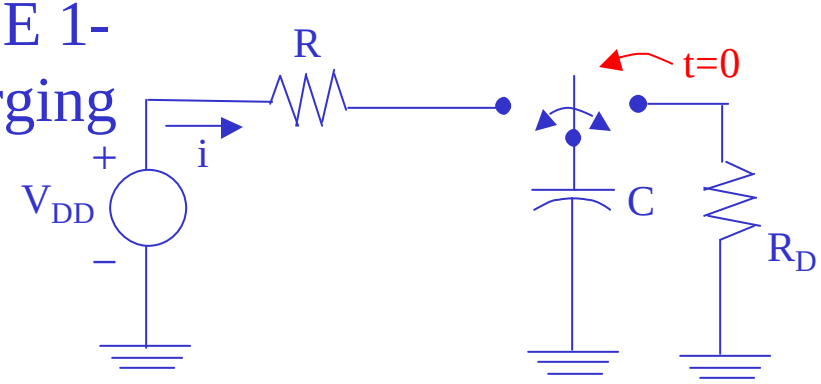
ENERGY AND POWER IN CHARGING/DISCHARGING CAPACITORS – A REVIEW

CASE 1- Charging



Capacitor initially uncharged ($Q=CV_{DD}$ at end)

Switch moves @ t=0

Power out of "battery"

$$P = i(t)V_{DD}$$

Energy out of "battery"

$$E = \int_0^\infty iV_{DD}dt = QV_{DD}$$

$$= CV_{DD}^2$$

Power into C

$$P_C = i(t)V_C(t)$$

Energy into C

$$E_C = \int_0^\infty iV_C dt$$

$$= \frac{1}{2}CV_{DD}^2$$

Power into R

$$P_R = [i(t)]^2 R$$

Energy into R (heat)

This must be difference of E and E_C, i.e. $\frac{1}{2}CV_{DD}^2$

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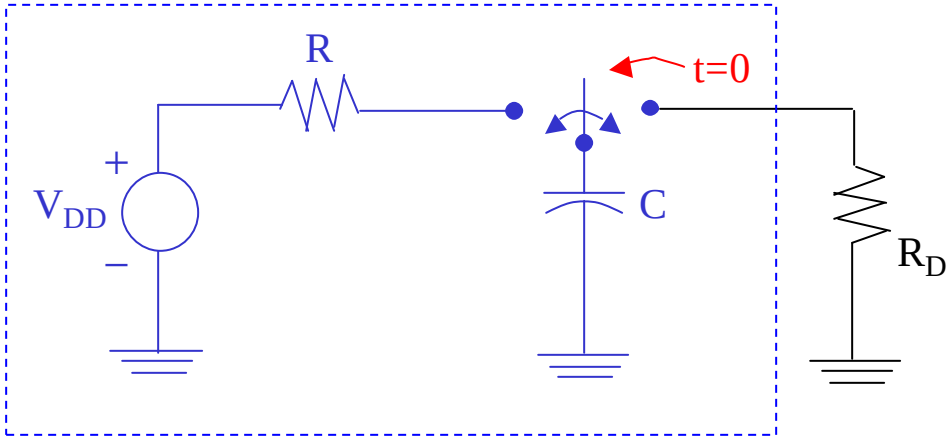
ENERGY AND POWER IN CHARGING



Capacitor initially uncharged ($Q=CV_{DD}$ at end)

Switch moves @ t=0

Energy out of "battery"

$= CV_{DD}^2$

Energy into C

$= \frac{1}{2} CV_{DD}^2$

Energy into R (heat)

$\frac{1}{2} CV_{DD}^2$

In charging a capacitor from a fixed voltage source V_{DD} half the energy from the source is delivered to the capacitor, and half is lost to the charging resistance, independent of the value of R.

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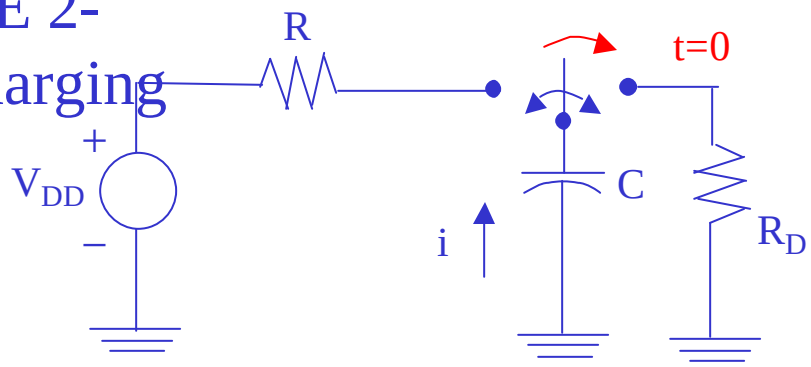
ENERGY AND POWER IN CHARGING/DISCHARGING CAPACITORS

CASE 2- discharging



Capacitor initially charged ($Q=CV_{DD}$) and discharges.

Switch moves @ t=0

Power out of battery

=0

Energy out of battery

=0

Power in/out of R

=0

Power out of C

$$P_C = i(t)V_C(t)$$

Energy out of C

$$E_C = \int_0^\infty iV_C dt = \frac{1}{2}CV_{DD}^2$$

Power into R_D

$$P_R = [i(t)]^2 R$$

Energy into R_D (heat)

This must be energy initially in C, i.e.

$$\frac{1}{2}CV_{DD}^2$$

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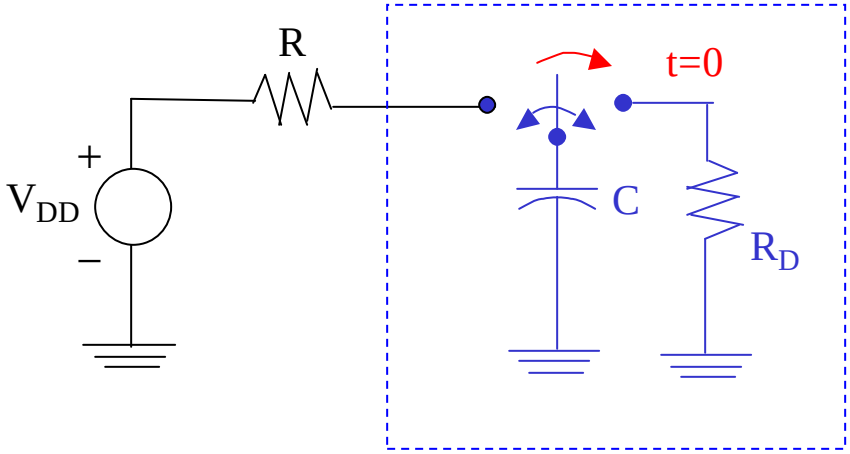
ENERGY IN DISCHARGING CAPACITORS



Capacitor initially charged ($Q=CV_{DD}$) and discharges.

Switch moves @ t=0

Energy out of C

$$= \frac{1}{2} CV_{DD}^2$$

Energy into R_D (heat)

$$\frac{1}{2} CV_{DD}^2$$

When a capacitor is discharged into a resistor the energy originally stored in the capacitor ($1/2\ CV_{DD}^2$) is dissipated as heat in the resistor

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POWER DISSIPATION in DIGITAL CIRCUITS

Each node transition (i.e. charging or discharging) results in a loss of $(1/2)(C)(V_{DD})^2$ How many transitions occur per second? Well if the node is pulsed up then down at a frequency f (like a clock frequency) then we have 2f dissipation events.

A system of N nodes being pulsed at a frequency f to a signal voltage V_{DD} will dissipate energy equal to $(N)\ (2f\ )(\frac{1}{2}CV_{DD})^2$ each second

Therefore the average power dissipation is $(N)\ (f\ )(CV_{DD})^2$

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LOGIC POWER DISSIPATION

Power = (Number of gates) x (Energy per cycle) x (frequency)

$$P = (N)\,(CV_{DD})^2\,(f)$$

N = 10^7; V_{DD} = 2 V; node capacitance = 10 fF; f = $10^9\ s^{-1}$ (1GHz)

P = 400 W! -- a toaster!

Pretty high but realistic

What to do? (N increases, f increases, hmm)

1) Lower V_{DD}
2) Turn off the clock to the inactive nodes

Clever architecture and design!

Lets define α as the fraction of nodes that are clocked (active). Then we have a new formula for power.

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LOGIC POWER DISSIPATION with power mitigation

Power = (Energy per transition) x (Number of gates) x (frequency) x fraction of gates that are active (α).

$$P = \alpha N f C V_{DD}^2$$

In the last 5 years V_{DD} has been lowered from 5V to about 1.5V. It cannot go very much lower. But with clever design, we can make α as low as 1 or 10%. That is we do not clock those parts of the chip where there is no computation being made at the moment.

Thus the 400W example becomes 4 to 40W, a manageable range (4W with heat sink, 40W with heat sink plus fan on the chip).