EECS 42

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PN junction diode, npn (and pnp) Bipolar Junction Transistor Modes of operation, the transistor as a switch, **COMPLEMENT** operation, DTL and TTL, DTL **NAND** gate, TTL **NAND** and **NOR** gates various addenda (Basics of Semiconductors).

Semiconductor Diode

Semiconductors are materials that are midway between conductors (very large or infinite conductivity – "zero" resistance) and insulators (almost no conductivity – "infinite" resistance). That is why they are sometime also called semiinsulators. Additions of some particular elements create either positive charge carriers (called holes – and the material called p-type) or negative charge carriers (electrons – and n-type semicond.) Typical semiconductor materials are, GaAs (gallium arsenide) Ge (Germanium) and the most common and well known SILICON, Si (sand is amorphous SiO_2 – abundance!).

A pn junction diode is a device formed by an n-type and a p-type semiconductor slabs in intimate contact.

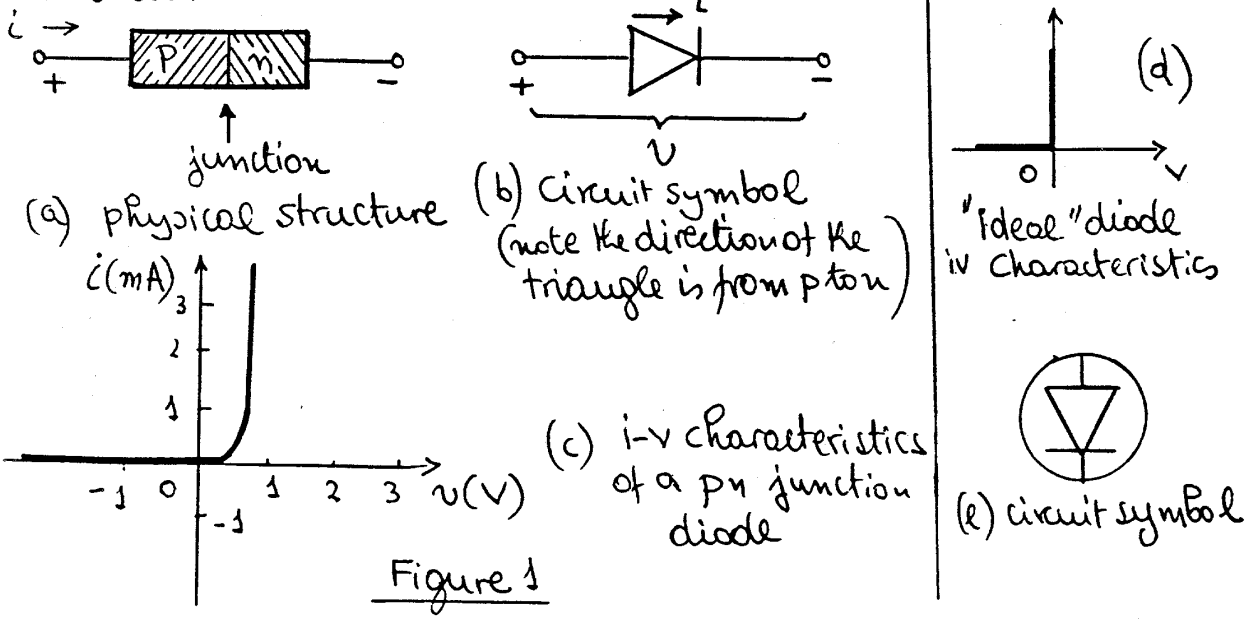
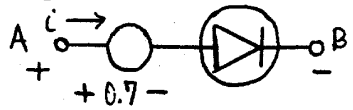


Figure 1

For our purposes a diode will have the following characteristics.
1. When current flows, $v = 0.7$ volts and 2. $i = 0$ (zero current flows) when $v < 0.7$V

So we can model a diode with a 0.7V ideal ind. voltage source in series with an "ideal" diode.



When $V_{AB} > 0$ → forward biased diode

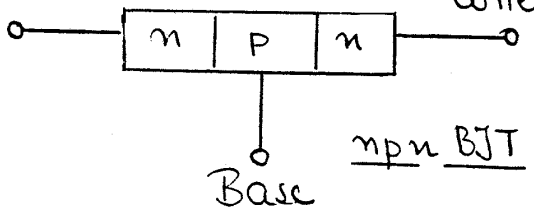
$V_{AB} < 0$ → reverse biased diode

Bipolar junction transistor (BJT)

A pn junction diode is an electronic device formed from the junction of a p-type semiconductor and an n-type semiconductor. If we add an extra junction (for example another n-type slab next to the p-type side) we get an npn bipolar junction transistor (BJT)
{The word bipolar implies that both holes and electrons take part in the operation of the device}.

Emitter

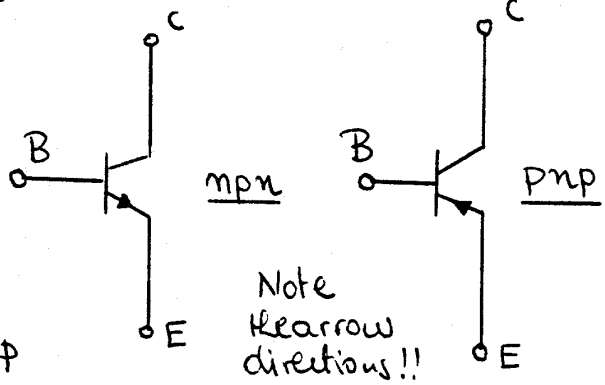
Collector



Base

npn BJT

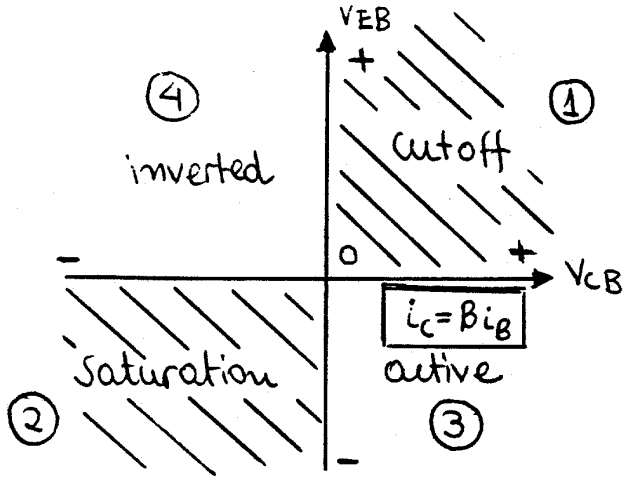
Circuit Symbols



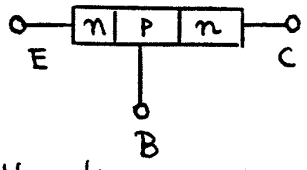
Note the arrow directions!!

Usually, all circuit equations hold true for either npn or pnp by just changing the polarities i.e. a positive V_{BE} becomes a negative V_{BE} and vise-versa. However, device constants might vary due to different values of the same parameters for electrons and holes.

The transistor may operate under various modes. There are four modes of operation: saturation, cutoff, active, and inverted (or inverted active mode). In saturation mode the transistor behaves like an ON switch, and in the cutoff mode like an OFF switch. Hence, in digital design we are only interested in those two, but switching from one to another, passes from the active regions, and also determines the speed of the switching operation.



an npn transistor under various modes of operation



physical model of npn transistor

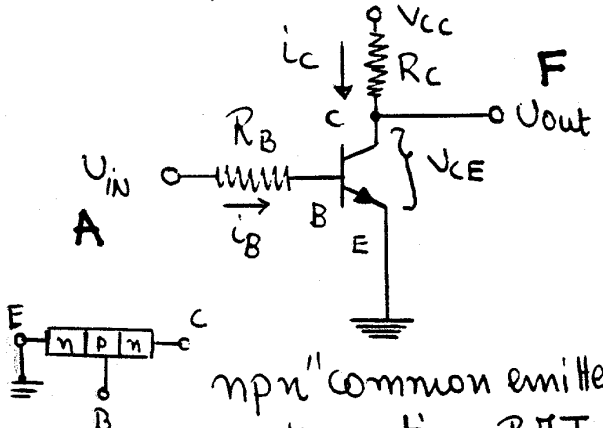
Cutoff mode

In region ① $\{ V_{EB} > 0, V_{CB} > 0 \}$ both junction diodes, i.e. EB and CB, are reversed biased. There is virtually no charge stored in the base region, and the collector current approaches zero. The cutoff mode corresponds to the open or OFF state of a transistor as a switch.

In region ②, Saturation mode, both junctions are forward-biased, and small voltages (biasing voltages) correspond to large output current. The transistor is in a conducting state and acts as a closed or ON switch.

Let us apply our introductory theory in trying to explain the use of a BJT performing a **COMPLEMENT** operation (i.e. **0→1** and **1→0**)

* { It is important to remember that (Figure 1, (c), page 1) that for a current $i = 1\,mA$, already the diode is forward biased and V is equal to 0.7 Volts.



npn "common emitter" configuration BJT

Inverter circuit

$V_{CC} = 5$ Volts

"High" range = 4 to 5 Volts

"low" range = 0 to 0.5 Volts

Case 1

V_{IN} is in the low range (i.e. $0 \le V_{IN} \le .5V$)

A=0

the BE diode is forward biased BUT since $V_{IN} < 0.7V$ no current flows ($i_B = 0$). Since, from transistor theory $i_C = \beta i_B \Rightarrow i_C = 0$

so, since the collector current is zero, no voltage drop across R_C, so $V_{out} = V_{CC} = 5$ Volts, i.e. in the "High" range and **F=1**.

Note that the transistor is actually in the cutoff region of the common-emitter configuration (see next page-Figure)

Before we tackle Case 2, let us emphasize that when in saturation v_{CE} approaches a minimum value in the neighborhood of 0.2V. This minimum value is referred to as V_{CEsat}. Also in saturation. i_B is greater than $\frac{i_c}{\beta}$

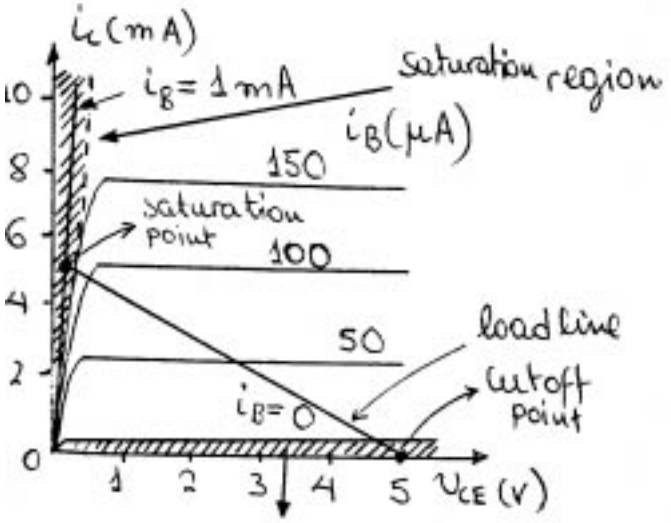
* { So in saturation 1. $v_{CE} = V_{CEsat} \cong 0.2$ Volts and 2. $i_B > \frac{i_c}{\beta}$

Case 2

v_{in} is in the "high" range, so the emitter-base junction is forward biased. The base current that flows is given approximately by:

$$i_B = \frac{v_{IN} - 0.7}{R_B}$$ where 0.7 volts is v_{BE} since forward biased.

If $i_B = 1$ mA and $v_{IN} = 4.5$V (A=1) we find $R_B = 3{,}800\Omega$.
(remember $V_{CC} = 5$ Volts)



For "ideal" case usually $i_B = 0$ coincides with the axis $i_c = 0$, so the cutoff region is just a one-dimensional line segment

Therefore the operating point is now at the intersection of the load line with the curve $i_B = 1$mA. With this large base current the transistor is now saturated. We see that when i_B is large, v_{CE} is small, and its value does not depend on the exact value of i_B. The value of v_{CE} is that of saturation $V_{CEsat} = 0.2$ Volts.

Thus Vout is in the "low" range

so **F = 0**

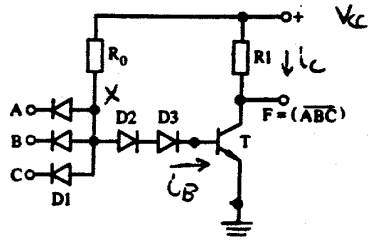
Again notice that when the transistor operates as a switch it operates either in the cutoff mode or the saturation mode. It is in the active region only during switching times

Since, as we have seen, it is possible to synthesize the other gates and flip-flops by connecting **NAND** gates together in different ways, it is appropriate to show how a **NAND** gates can be produced with diodes and transistors (DTL - diode-transistor logic) or only with transistors (TTL - transistor-transistor logic).

DTL NAND gate

For simplicity let us assume that we have only two inputs **A** and **B**

$V_{cc}=5$ Volts



Case 1.

both v_A and $v_B = 0$ Volts (low range)
So most probably both diodes A and B conduct so $v_X = .7$ Volts. However D_2 D_3 and BE (base-emitter diode) need $3 \times 0.7 = 2.1$ Volts in order to have conduction. So since $v_X = .7V < 2.1$ Volts $i_B = 0$ which also implies $i_C = 0 \Rightarrow v_F = V_{cc} = 5V$ i.e. **A = 0, B = 0 and F = 1**

Case 2.

either v_A or v_B is "high" (=4.5 volts) and the other "low" $\{$ **A = 1, B = 0** or **A = 0, B = 1** $\}$

let us assume $v_B = 4.5$ Volts and $v_A = 0$ Volts.

Since $\max (V_{cc} - v_B) = .5$ Volts diode B does not conduct.
So diode A conducts $\Rightarrow v_X = .7V < 2.1V$ so $v_F = 5V$ and **F = 1**

Case 3.

both v_A and v_B in the "high" range, i.e. equal to 4.5 Volts. Neither diode A or diode B conduct. $V_X = 2.1$ and base current flows in the transistor so we have saturation and $v_F = v_{CE} = V_{CEsat} = 0.2$ V (low range)
i.e. **A = 1, B = 1 $\Rightarrow$ F = 0**

So we conclude that $F = \overline{AB}$

TTL NAND gate

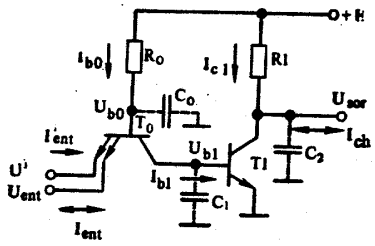


Fig. Porte ET-NON en TTL à inverseur simple

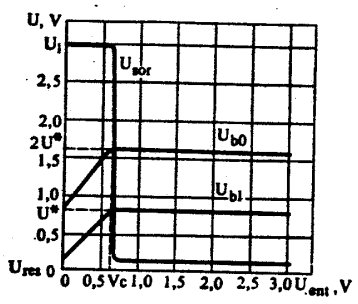


Fig. - Caractéristique de transfert typique et variation des tensions sur les bases des transistors T_0 et $T1$ en fonction du potentiel U_{ent} pour $E = 3$ V, $T = +20$ °C, $n = 1$

TTL NOR gate