12/04/03 more device equations

EECS 42 – Introduction to Digital Electronics

Fall 2003, Prof. A. R. Neureuther
Dept. EECS, 510 Cory 642-4590
UC Berkeley Office Hours During Finals Listed Below
Course Web Site http://www-inst.EECS.Berkeley.EDU/~ee42/

Topical Coverage Final Exam

8-11 AM Friday, December 12 room TBA

Closed Book – Device Equations Provided

Bring Calculator, Paper provided

Review Session (3:30-5 PM), Wednesday, December 10th, 289 Cory

Review Session (3:30-5 PM), Thursday, December 11th, 289 Cory

Office Hours: 8th 11 IS, 9th 11 EC & 3:30 EC, 10th 11 IS, 11th 11 AN

Schwarz and Oldham Material followed by skills

Chapter 2: all except 2.4 Loop Analysis, 2.6 and 2.7, light on 2.5
Node analysis of circuits with up to 8 branches, Voltage and current dividers

Chapter 3: all
Equivalent circuits: Thevenin and Norton; Nonlinear loads and load lines

Chapter 4: all but only ideal op-amps
Dependent sources, gain, input and out put impedance; Ideal Op-Amps; **Comparators (L15)**.

Chapter 5: all light on 5.3 and very limited inductor circuits.

Chapter 8.1: Only 8.1 EE 40/42 solution method; KCL to get differential equation; pulses

Chapter 10: no flip-flops Gates and logic functions; Timing diagrams (L12)

Lectures 16-17, O&S pp. 522-524, 604-611 Static Logic with state dependent devices
Device I vs. V curves and load line method; Static Power; Simple inverter and voltage transfer function; Complementary Pull-Up and Pull-Down (CMOS)

Lectures 18-22 O&S pp. 604-618 and viewgraphs: Dynamic Logic
Dynamic (Transient) Switched Resistor Model and 0.69RC delay;
Worst case propagation delay, Cascade propagation delay
Use of Latches and designing clock delay

Lectures 23-24, O&S pp. 481-499, 511-527, 594-598, Device physics and models
Diode equation, perfect rectifier and large signal models and use in circuits.
Carrier motion as basis for conductance and conductance-resistance of MOS

Likely Exam Emphasis

Transient
Logic Functions and Timing Diagrams
Dependent Sources, Gain, Thevenin resistance
Ideal Op-Amps,
Load Lines and Static analysis of logic gates using I vs. V model
CMOS Logic Functions, Delay, Latches
Diode circuit analysis and signal processing, Gate controlled resistance

EE 42 Device

$$I_{OUT-SAT-D} = k_D\left(V_{IN} - V_{TD}\right)V_{OUT-SAT-D}$$

$$I_{OUT-SAT-U} = k_U\left(V_{DD} - V_{IN} - V_{TU}\right)V_{OUT-SAT-U}$$

When in circuit attached to V_{DD}.

$$\sigma = qN\mu \qquad R = \frac{L}{\sigma \cdot h \cdot w} = \left(\frac{1}{\sigma \cdot h}\right)\left(\frac{L}{W}\right) = R_{SHEET}\left(\frac{L}{W}\right)$$

$$k_D = \mu_n C_{OX}\left(\frac{W}{L}\right)_n \qquad \mu_n = 500\left(cm^2/Vs\right) \qquad \mu_p = 150\left(cm^2/Vs\right)$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\left(8.85x10^{-14}\,F/cm\right)(3.9)}{6x10^{-7}\,cm} = 5.75x10^{-7}\,F/cm^2$$