11/02/03

EECS 42 – Introduction to Electronics for Computer Science

Fall 2003, Prof. A. R. Neureuther
Dept. EECS, 510 Cory 642-4590
UC Berkeley OH M 1, Tu-Th 10:30=11:30, F 11
Course Web Site http://www-inst.EECS.Berkeley.EDU/~ee42/

Midterm Thursday November 6th
In class, Closed Book, Closed Notes, Device Equations Provided
Review Session #1: 5 PM Tuesday Nov 4th, meet at 241 Cory
Review Session #2: 6 PM Wednesday Nov 5th, meet at 241 Cory

Topical Coverage Second Midterm

Schwarz and Oldham Material followed by skills

Chapter 2: all except 2.4 Loop Analysis, 2.6 and 2.7, light on 2.5
- Node analysis of circuits with up to 8 branches
- Voltage and current dividers

Chapter 3: all
- Equivalent circuits: Thevenin and Norton
- Nonlinear loads and load lines

Chapter 4: all but only ideal op-amps
- Dependent sources, gain, input and out put impedance
- Ideal Op-Amps
- **Generalization to Comparators**

Chapter 5: all light on 5.3 and no inductor circuits.

Chapter 8.1: Only 8.1
- EE 40/42 simple solution method and application to switching and pulses
- KCL to get differential equation for capacitor voltage and inductor current

Chapter 10: no flip-flops
- Gates and logic functions
- **Generalization: Timing diagrams**

Lectures 15-18, pp. 522-524, 604-611 Logic with state dependent devices
- Device I vs. V curves and load line method
- Simple inverter and voltage transfer characteristic
- Complementary Pull-Up and Pull-Down networks (CMOS)

Likely Exam Emphasis

Analysis of vanilla circuits with dependent sources
Ideal Op-Amps
Analysis of circuits using dependent sources to improve characteristics
Logic Functions and Timing Diagrams
Static but no dynamic analysis of logic gates

$$I_{OUT-SAT-n} = k_n'\left(\frac{W}{L}\right)_n (V_{IN} - V_{Tn})V_{OUT-SAT-n}$$

$$I_{OUT-SAT-p} = k_p'\left(\frac{W}{L}\right)_p (V_{DD} - V_{IN} - |V_{Tp}|)V_{OUT-SAT-p}$$

	V_T(V)	$V_{OUT-SAT}$ (V)	k' (μA/V²)
NMOS	0.43	0.63	100
PMOS	0.4	1	25

For a minimum sized device W/L =2