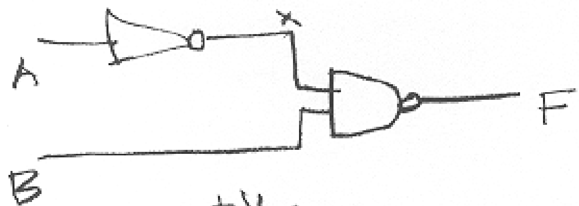

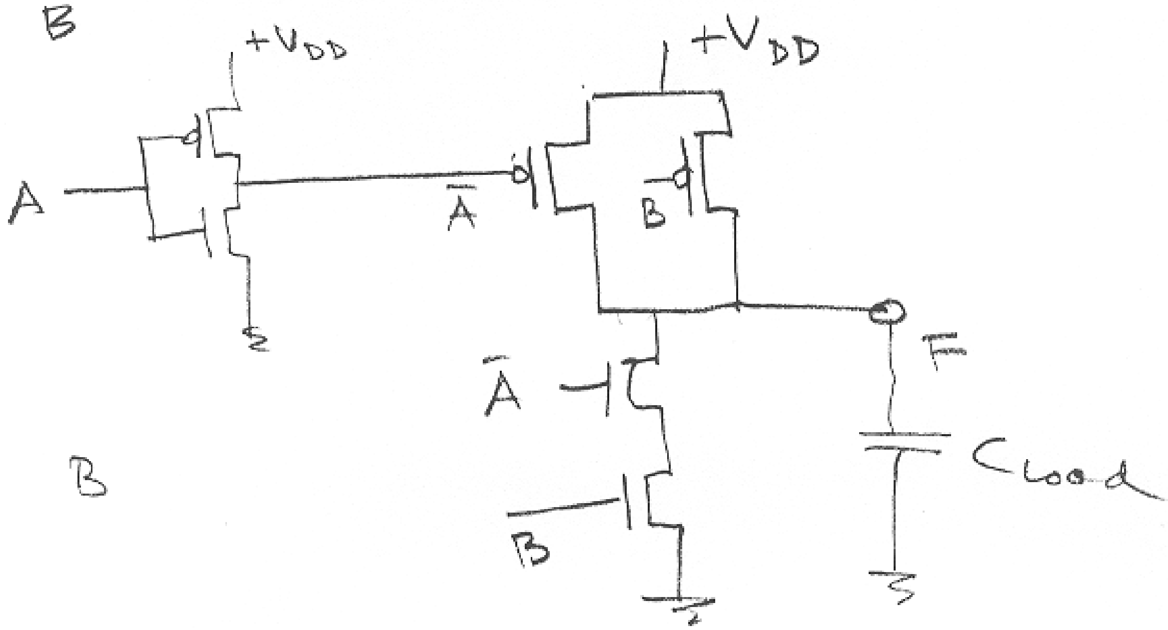

a. $F = \overline{(\overline{A} \cdot B)}$

b. Truth table

A	$\overline{A}$	B	F
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1

c. $C_G = C_{ox} \cdot$ gate electrode area $= C_{ox} \cdot W \cdot L$

$C_{ox} = 2{,}3\ fF/\mu m^2$

use Ws and Ls as on diagram in notes of 29.04.02 (see second page), i.e.,

PMOS 12 µm and 1.5 µm

NMOS 6 µm and 1.5 µm

Let R_P ═══, $R_N = 4\ k\Omega$

Find $C_{GP} = 2.3fF \cdot 12 \times 1.5 = 41.4 fF$

$C_{GN} = 2.3fF \cdot 6 \cdot 1.5 = 20.7 fF$

d. What is fanout of the inverter (1)

e. What gate capacitance does the inverter drive?

$$C_{GP} + C_{GN} = 41.4 + 20.7 = 62.1 fF$$

f. In NAND gate what is the source resistance when F goes from 1 to 0?

$$R = 2R_N = 8k\Omega$$

g. In NAND gate what is the maximum resistance when F goes from 0 to 1?

max if only one PMOS ~~is also~~ changes state → $4k\Omega$

h. ~~In terms of R_P and R_N, and~~ what is the time delay in the inverter?

$$\tau_{inv} = R(C_p + C_N) = 4k\Omega(62.1 fF) = 248 ps$$

gate delay $= 0.69\tau = 171 ps$

i. If the load capacitance $C_L = 100 fF$, what is the maximum delay in the NAND gate? $\tau_{max} = R_{max} \cdot C_L = 8k\Omega \cdot 100 fF = 800 ps$; delay $= 0.69\tau = 552 ps$

i. What values of A, B ... to this?

K. If A goes from a 0 to a 1 ~~how~~
~~much~~ energy is stored in ~~the~~ one gate
~~of inverter~~ capacitance of the inverter.

L. Which one (PMOS or NMOS)? <u>NMOS</u>
~~How~~ much energy (assuming $V_{DD} = +5V$

$$U = \frac{1}{2}CV^2 = \frac{1}{2}(20.7fF)(25)$$

$$= 2.6 \times 10^{-13}\ J$$

M. If change occurs once each clock cycle in a 500MHz ~~clo~~ processor, how much power is expended?

$$P = U \cdot f = 2.6 \times 10^{-13} \times 5 \times 10^{8} =$$

$$129 \mu W$$

N. If there are
60 watts → $\frac{60}{129 \times 10^{-6}}$ = 464,000 gate