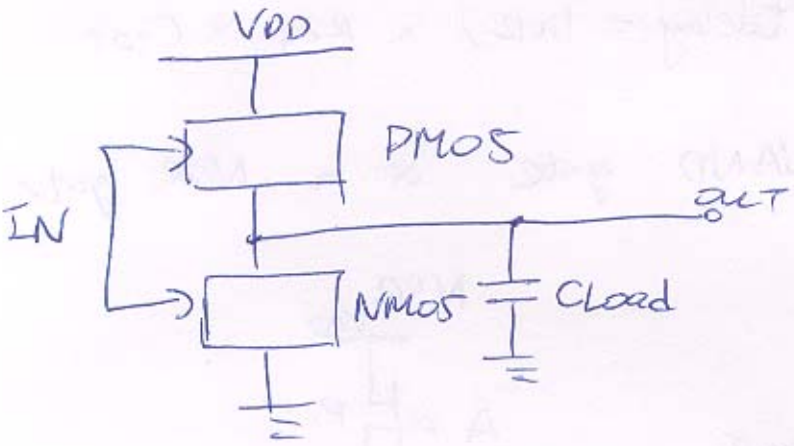
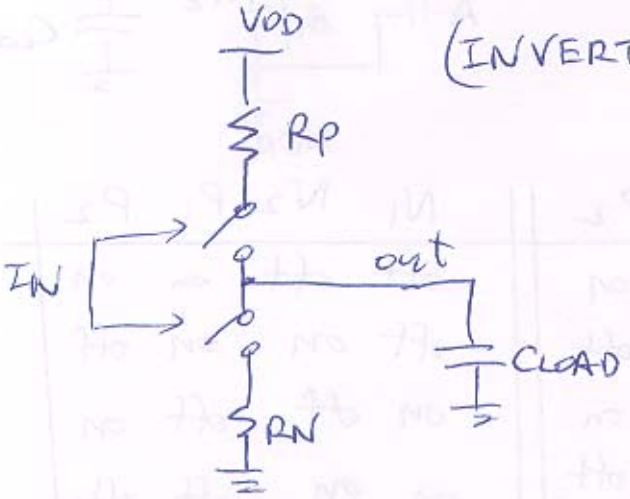
EE42 REVIEW (eddieng@eecs)

CMOS Digital Gates:



$C_{load} = C_{wire} + C_{gate\_total}$ (of next logic gates)

(INVERTER)

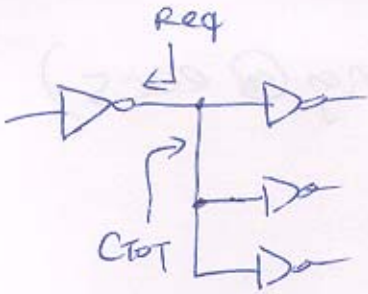


① IN (L → H)
OUT (H → L)
NMOS (off → on) ⇒ RN
PMOS (on → off)

$t_{delay} = \ln(2) \times R_N \times C_{LOAD}$

② IN (H → L)
OUT (L → H)
NMOS (on → off)
PMOS (off → on) ⇒ Rp

$t_{delay} = \ln(2) \times R_p \times C_{LOAD}$



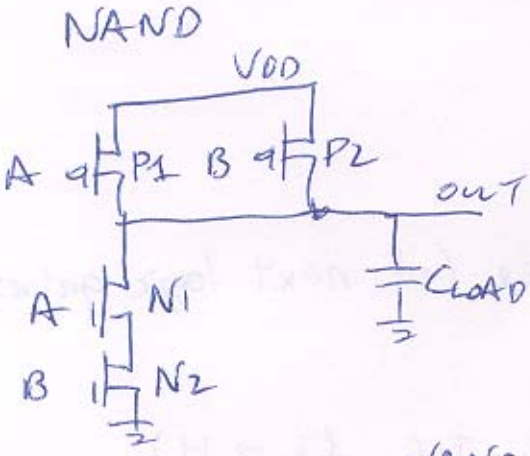
FO = 3

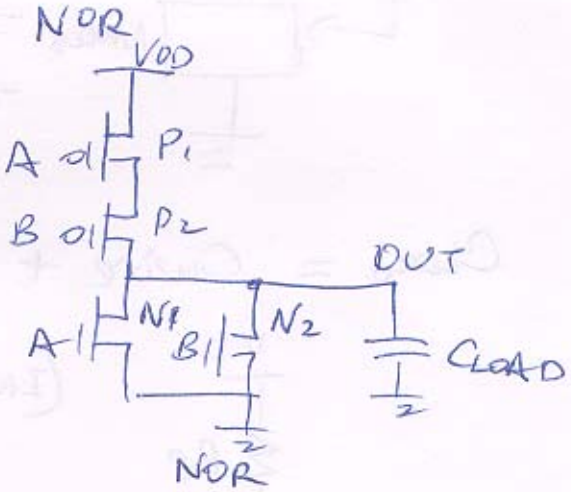
$C_{TOT} = C_{wire} + 3(C_{gp} + C_{gN})$

$R_{eq} = R_N$ or R_p.

$t_{delay} = \ln(2) \times R_{eq} \times C_{TOT}$

What about a NAND gate or a NOR gate?





NAND

AB	N_1	N_2	P_1	P_2
00	off	off	on	on
01	off	on	on	off
10	on	off	off	on
11	on	on	off	off

AB	OUT	Req
00	1	$R_p // R_p$
01	1	R_p
10	1	R_p
11	0	$R_N + R_N$

NOR

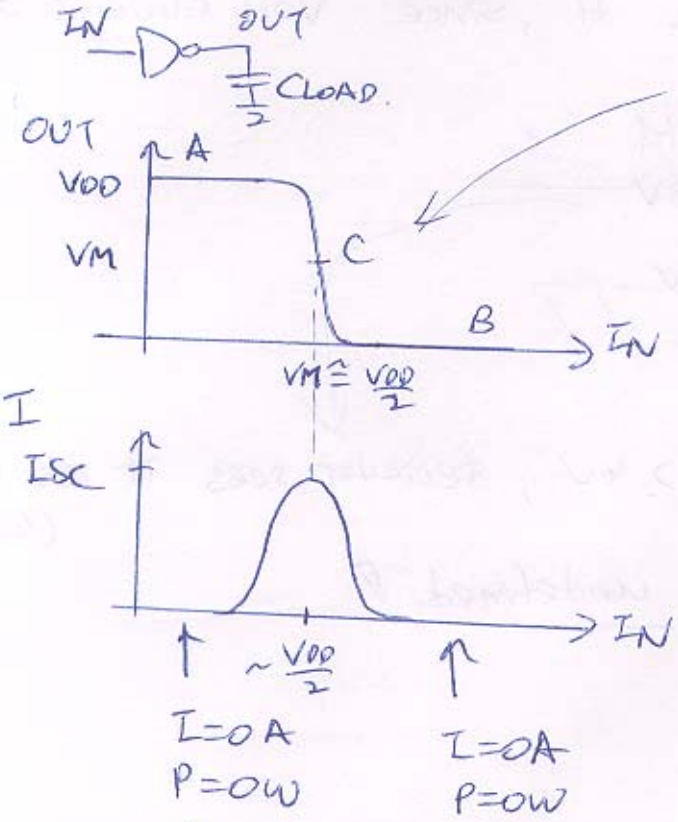
N_1	N_2	P_1	P_2
off	off	on	on
off	on	on	off
on	off	off	on
on	on	off	off

OUT	Req
1	$R_p + R_p$
0	R_N
0	R_N
0	$R_N // R_N$

What about XOR, AND, OR and XNOR gates?

(These are good exercises for practice!)

Voltage Transfer Characteristic



how can we make inverter operates at point C ?

3 stable operating points A, B & C.

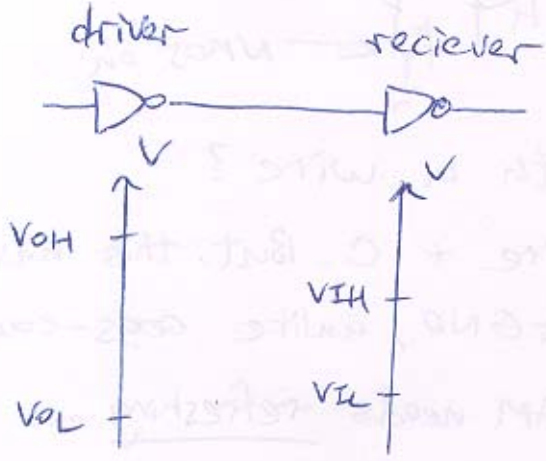
- points A & B are used for digital logic level.
- point C should be avoided!! (because it draws a lot of static power = $I_{SC} \times V_{DD}$)

Very attractive property of CMOS → No power dissipation when idle !!

Switching power = $(C_{LOAD})(V_{DD}^2)(\text{frequency})$ [units of W]

Energy stored = $\frac{1}{2} C_{LOAD} V_{DD}^2$ [units of J]

Noise Margin

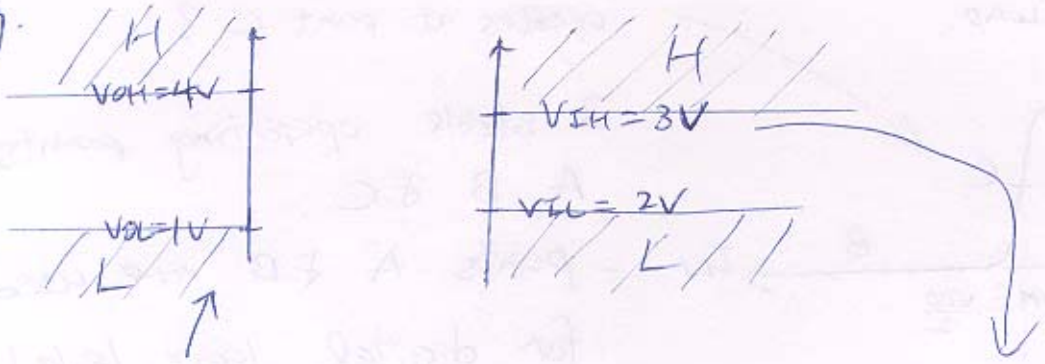


$NM_H = V_{OH} - V_{IH}$

$NM_L = V_{IL} - V_{OL}$

Driver outputs H > V_{OH} such that reciever recognizes that as logic H, since V_{OH} always > V_{IH}.

e.g.

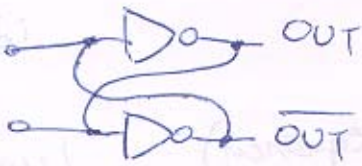


since logic H voltage > 4V, reciever sees it as H (4V > 3V)

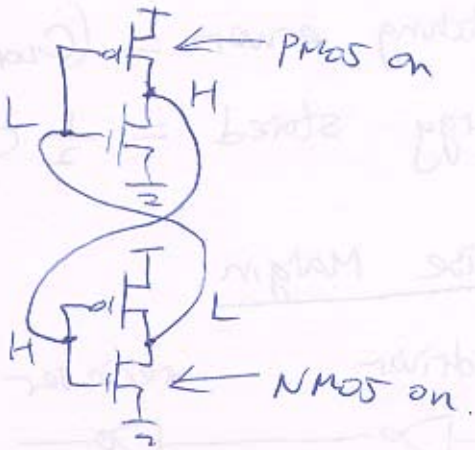
Level in between is undefined!

Sequential logic

Has memory through feedback...



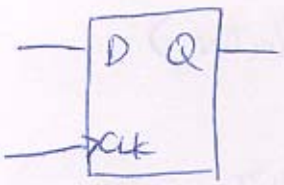
OUT = H, $\overline{OUT}$ = L



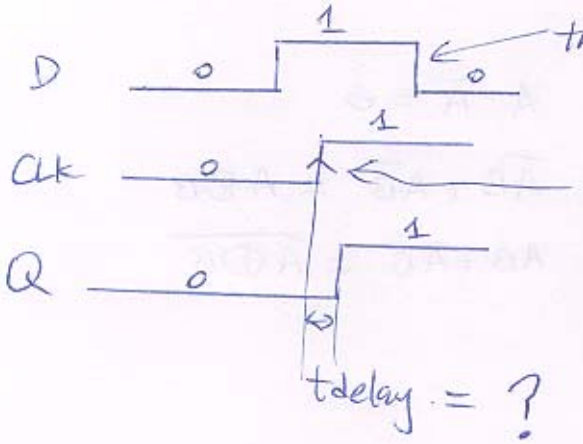
Can you replace this with a wire?

DRAM is essentially a wire + C. But this has no direct path to VDD & GND, unlike cross-coupled inverters or SRAM! DRAM needs refreshing...

D Flip-Flop



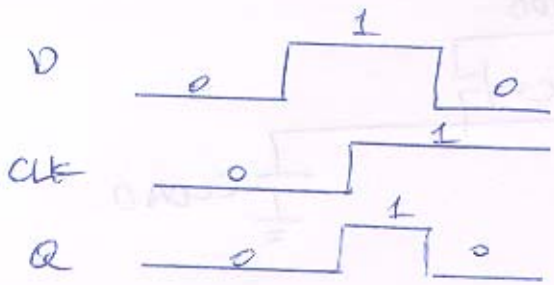
↳ this is edge trigger ⇒



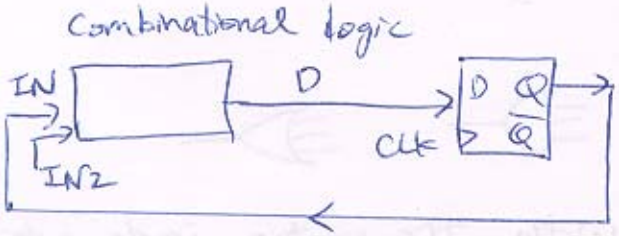
this will not cause Q to change since there is no edge in clock!

this edge looks at value of D; Q changes as a result.

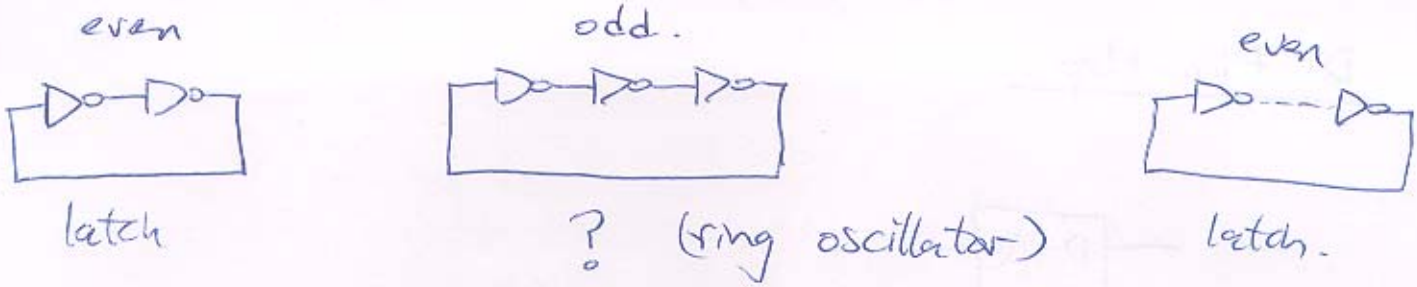
Latch is level sensitive

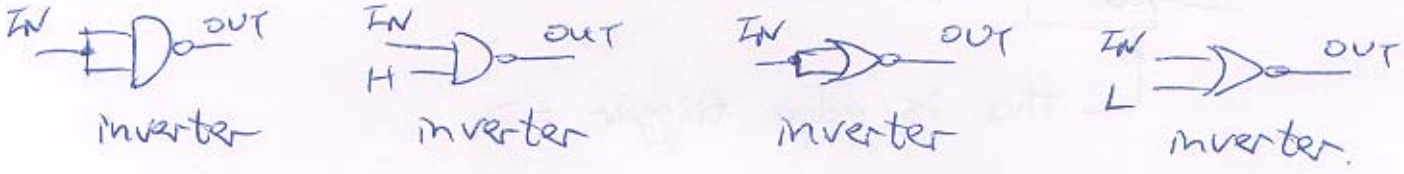


Q follows D when clk = 1.



D depends on IN2 & Q (from previous cycle!)





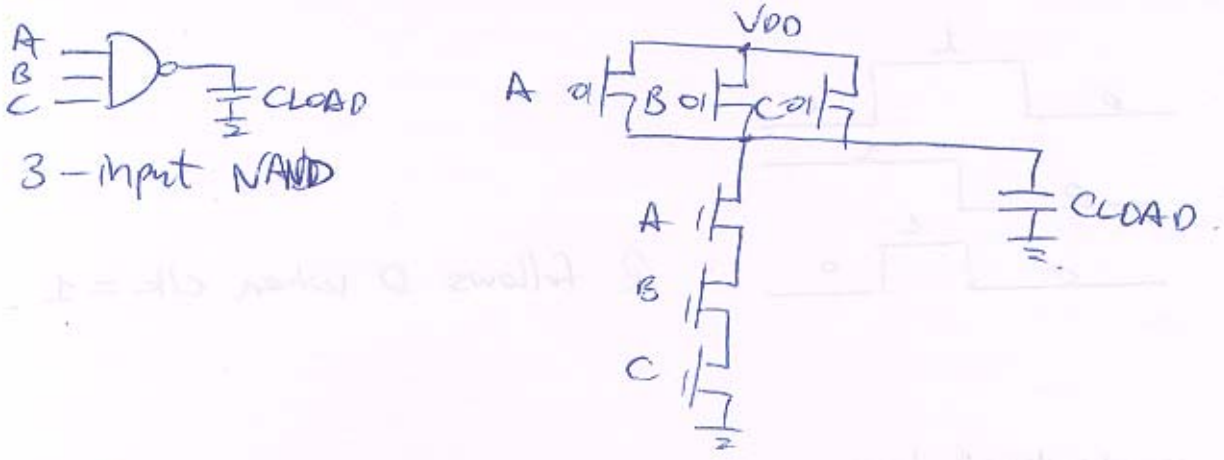
$1 \cdot A = A$ $\quad A \cdot A = A$ $\quad A \cdot \bar{A} = 0$

$1 + A = 1$ $\quad A + A = A$ $\quad \bar{A}B + A\bar{B} = A \oplus B$

$0 + A = 0$ $\quad A + \bar{A} = 1$ $\quad AB + \bar{A}\bar{B} = \overline{A \oplus B}$

$\overline{AB} = \bar{A} + \bar{B}$ (De Morgan's)

$A + B = \overline{(\bar{A}\bar{B})}$



Try to come up with transistor implementation of these 3-input gates!