PRACTICE PROBLEMS

(eddieng@eecs)

Draw logic gates implementation of the following equations

1, $F = AB \oplus C$, "$\oplus$" = XOR

2, $G = A\bar{B} + (\bar{C} + D)(E)$

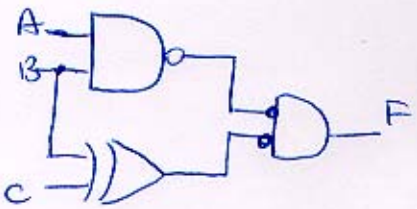
3, $F = A\bar{B} + ABC$

4, $G = \bar{X}Y\bar{Z} + YZ + \bar{Y}X$

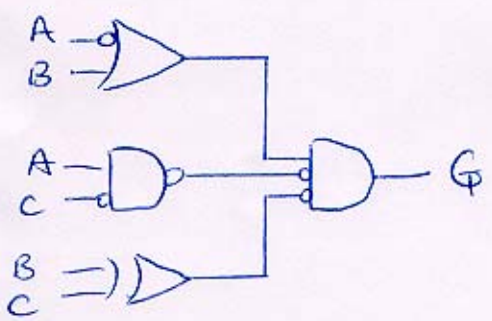
5, $F = \overline{(X \oplus \bar{Y})(\bar{Z})}$

Derive Boolean equations from the following circuits and simplify results if you can:

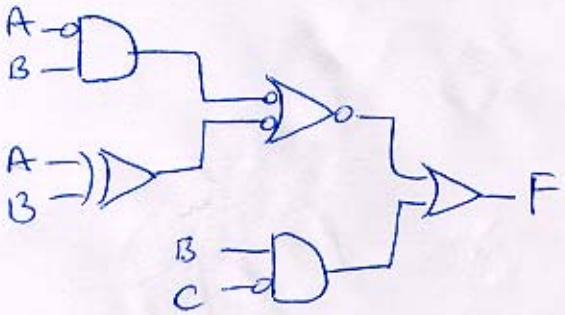
6,



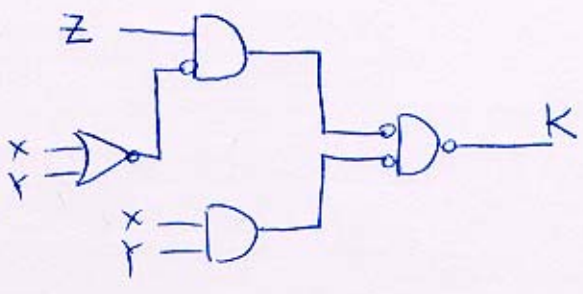
7,

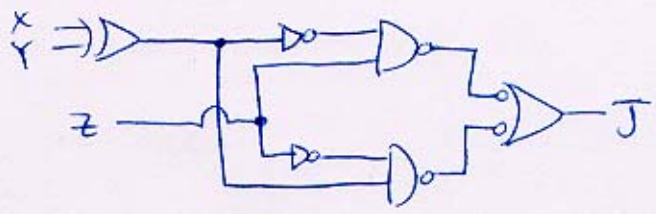


8,



9,





10, Obtain Boolean equations from the turth table:

inputs outputs : I, J, K, L, M, N

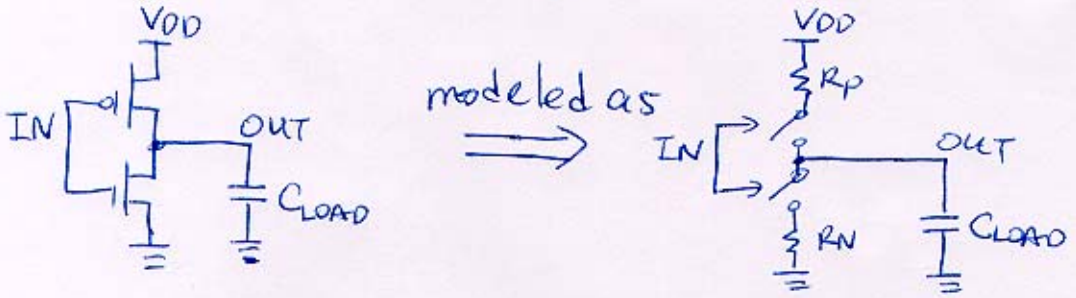
X Y Z	I	J	K	L	M	N
0 0 0	0	0	1	1	0	0
0 0 1	0	1	1	0	0	1
0 1 0	0	1	1	1	0	1
0 1 1	0	0	1	1	0	1
1 0 0	0	1	1	0	1	1
1 0 1	0	0	1	0	0	1
1 1 0	1	0	1	1	0	1
1 1 1	1	1	1	0	1	1

11, a, Consider $F = (A+B)\cdot C$. Draw function F using one OR gate and one AND gate.

b, Draw F using <u>only</u> NOR gates. (Hint: use De Morgan's Theorem)

c, Draw F using <u>only</u> NAND gates.

12, Consider the following inverter:



If $R_p = 1.5k\Omega$, $R_N = 1.0k\Omega$, $C_{Load} = 1pF$, what is the delay from IN to OUT when OUT is making a low to high transition? A High to low transition? What is the average?