



# EECS 42 – Introduction to Electronics for Computer Science

Fall 2001,  
Dept. EECS,  
UC Berkeley  
Course Web Site <http://www-inst.EECS.Berkeley.EDU/~ee42/>

Prof. A. R. Neureuther  
510 Cory 642-4590  
Tentative OH M, Tu, W, (Th), F 11

## Midterm #2 November 7th, 2001

**Closed Book, Closed Notes**  
**Write on the Exam paper**

**Print Your Name:** \_\_\_\_\_

**Sign Your Name:** \_\_\_\_\_

**Show your work so that the method as well as the answer can be graded for correctness and completeness. Correct answers alone are only worth 70% of full credit.**

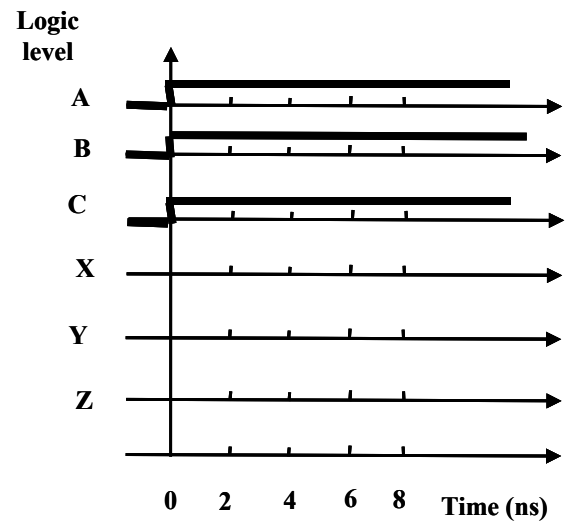
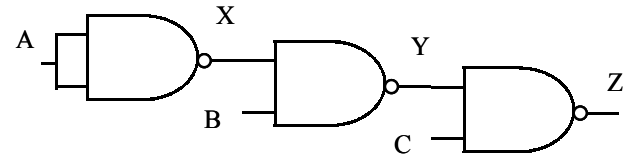
Problem	Possible	Score
I	30	
II	25	
III	22	
IV	23	
<b>Total</b>	<b>100</b>	

### I (30 Points) Logic and Timing Diagrams

Inputs A, B, and C have all been zero (low) for a long time and then at  $t = 0$ , A, B and C go to (high) for a long time.

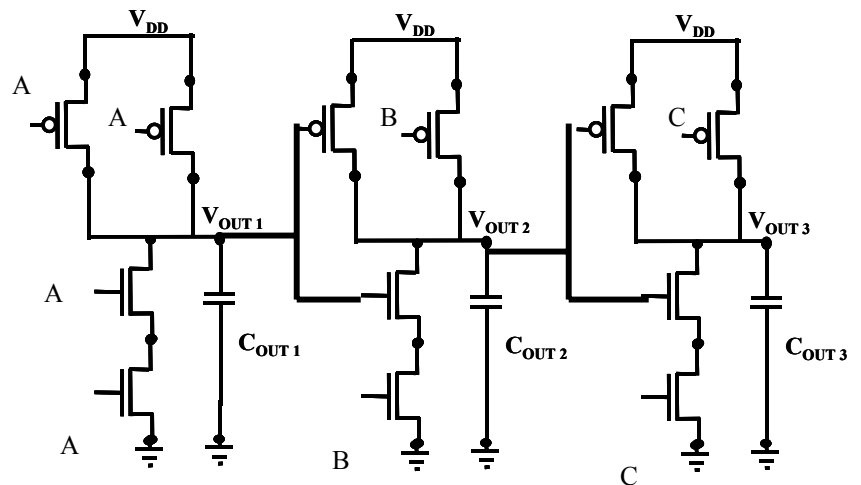
- a) (5 Points) Find the values of X, Y and Z just before  $t = 0$ , and then as  $t$  goes to infinity.

	Before $t=0$	As $t \Rightarrow$ infinity
X		
Y		
Z		



- b) (10 Points) Complete the timing diagram to the right assuming that each gate has a propagation delay of 2 ns before the correct output appears at its output.

- c) (7 Points) For the CMOS circuit implementation to the right of the NAND gate logic circuit above and the signal changes in part a), **find the time at which the change reaches  $V_{OUT1}$** . State the delay in terms of  $0.69RC$  using  $R_U$  and  $R_D$  (from the switched resistor device models) and the capacitors shown.

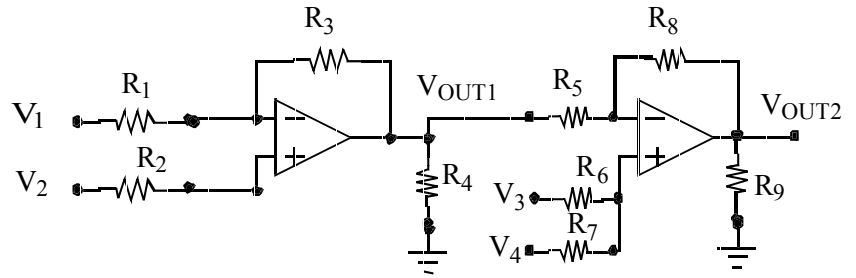


- d) (8 Points) For the CMOS circuit implementation to the right of the NAND gate logic circuit above and the signal changes in part a), **find the time at which the change reaches  $V_{OUT3}$** . State the delay in terms of combinations of  $0.69RC$  using  $R_U$  and  $R_D$  (from the switched resistor device models) and the capacitors shown.

## II (25 Points) Ideal Op-Amp Analysis

Use the ideal op-amp analysis method in this problem.

- a) (8 Points) Find  $V_{OUT1}$  in terms of the resistances and input voltages.



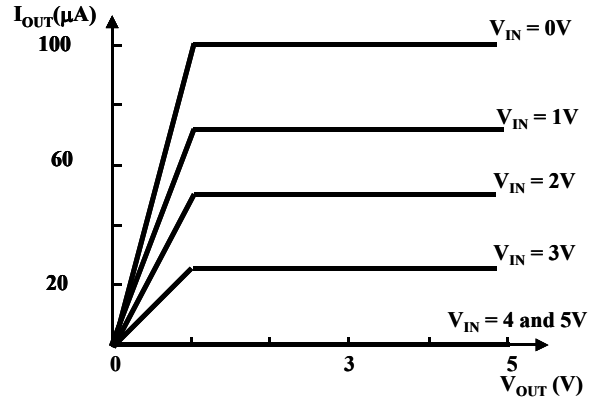
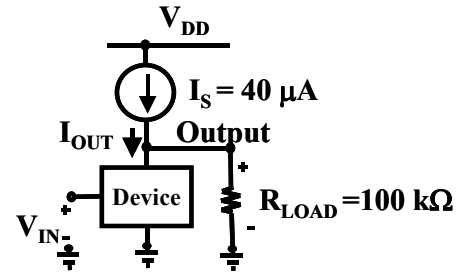
- b) (9 Points) Give sufficient additional equations for finding  $V_{OUT2}$  in terms of the resistances and input voltages. Do not solve.

- c) (8 Points) Assume that  $V_{OUT2} = k_1V_1 + k_2V_2 + k_3V_3 + k_4V_4$ . For  $i = 1,4$  complete the table below by determining the sign of  $k_i$  and listing the resistors that will contribute to  $k_i$ . Hint: Start with what you know from part a) to reach  $V_{OUT1}$  and then apply this principle again.

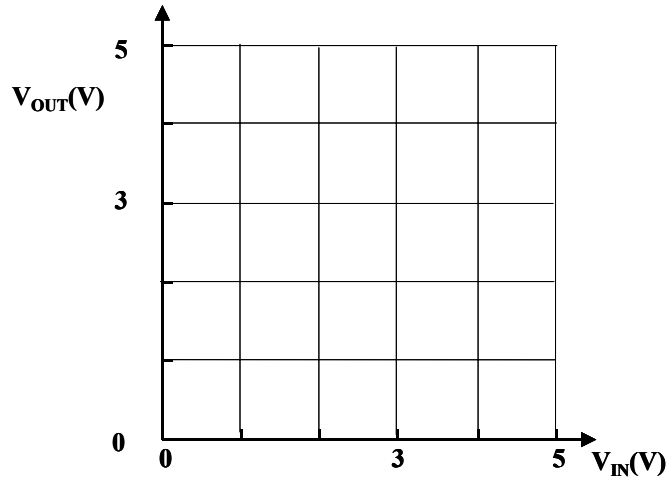
Term number i	Sign of $k_i$	Resistors Contributing to $k_i$
V1		
V2		
V3		
V4		

### III (22 Points) Device I vs. V Curves

- a) (10 Points) For the logic circuit and device characteristics shown find  $V_{OUT}$  when  $V_{IN} = 3V$ .

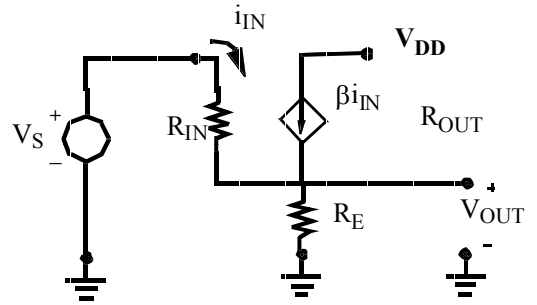


- b) (12 Points) For the logic circuit shown, approximately sketch the voltage transfer function  $V_{OUT}$  vs.  $V_{IN}$ . Specify values of  $V_{OUT}$  for  $V_{IN} = 0, 3$  and  $5V$ .



#### IV (23 Points) Advanced Circuits with Dependent Sources

a) (10 Points) Find  $V_{OUT}/V_{IN}$ .



b) (13 Points) Find the Thevenin resistance looking into the output.