# EECS 42 – Introduction to Electronics for Computer Science

Fall 2001, Prof. A. R. Neureuther
Dept. EECS, 510 Cory 642-4590
UC Berkeley Tentative OH M, Tu, W, (Th), F 11
Course Web Site http://www-inst.EECS.Berkeley.EDU/~ee42/

## Final Examination December 14th, 2001

## Closed Book, Closed Notes
## You may use the equation sheet provided.
## Write on the Exam paper

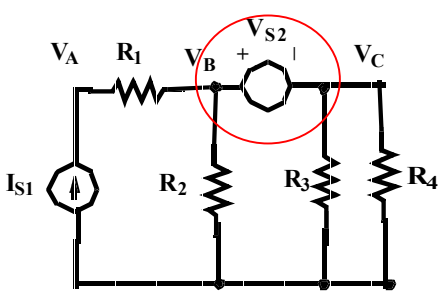
## Print Your Name:_____Solutions_____

## Sign Your Name:_____

**Show your work so that the method as well as the answer can be graded for correctness and completeness. Correct answers alone are only worth 70% of full credit.**

| Problem | Possible | Score |
|---|---|---|
| I | 42 | |
| II | 38 | |
| III | 40 | |
| IV | 38 | |
| V | 42 | |
| Total | 200 | |

**I (42 Points) Basic Circuit Concepts**

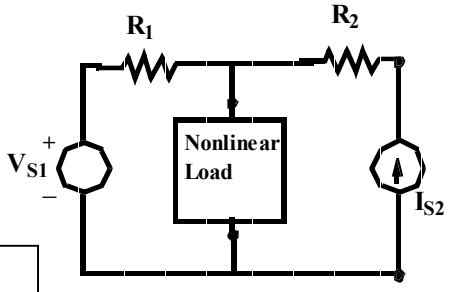


a) (10 Points) Find a single equation for $V_C$ in terms of $I_{S1}$, $V_{S2}$ and the resistors.

Use bag around $V_{S2}$ and apply KCL.

$$-I_{S1}+\frac{(V_C-V_B-0)}{R_2}+\frac{(V_C-0)}{R_3}+\frac{(V_C-0)}{R4}=0$$

b) (10 Points) Find the Thevenin equivalent circuit seen looking outward from the nonlinear device.

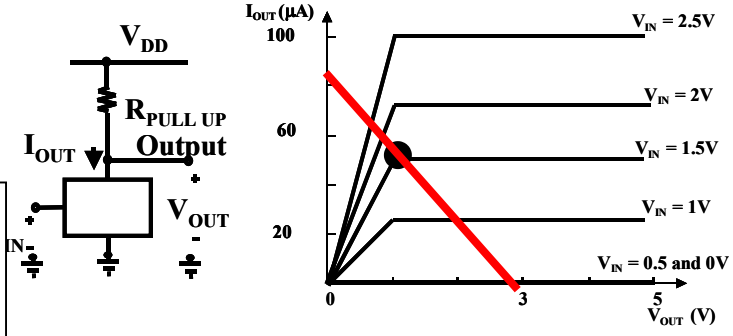



$V_{OC} = V_{S1} + I_{S2}R_1$

$R_{TH} = R_1$

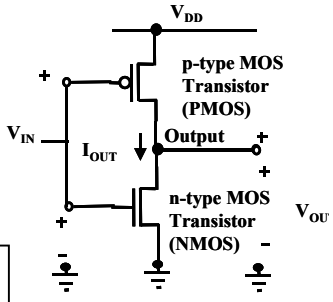
Turning the sources to zero makes $I_{S2}$ and open circuit.

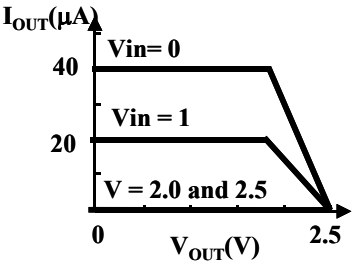
c) (10 Points) Specify a value of R, $V_{DD}$ and $V_{IN}$ that makes the circuit operate at the point indicated on the I vs. V for an NMOS device.

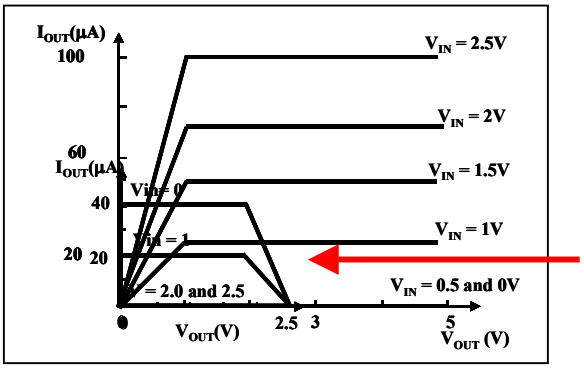



Example: The input must be 1.5 volts to select the correct curve. Assume $V_{OC}$ = 3V and draw a straight line through the point given. It hits the vertical axis at 84 µA. Thus $R_{TH}$ = (3V/84 µA) = 35.7kΩ.

d) (12 Points) Graphically estimate $V_M$ and the short circuit current when the PMOS with the I vs. V to the right and NMOS with I vs. V above are combined to create a CMOS inverter with $V_{DD}$ = 2.5V.



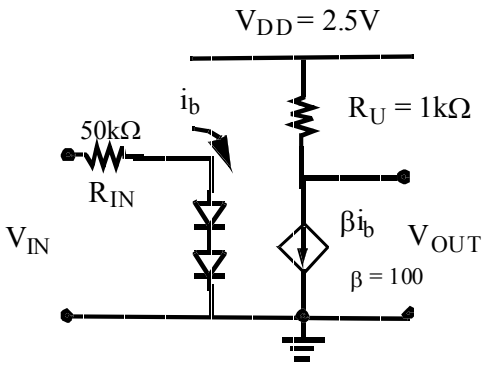




Before $V_{IN}$ reaches 1.0 volt the intesection switches from $V_{OUT}$ high to $V_{OUT}$ low. Thus $V_M$ is about 0.9V and the current, which is the short-circuit current is about 22 µA.

## II (38 Points) Dependent Sources

a) (6 Points) Using the large signal diode model, find $i_b$ when $v_{IN}$ is 2V.




$$i_b = \frac{(V_{IN} - 0.7V - 0.7V)}{R_{IN}} = \frac{(2.0V - 0.7V - 0.7V)}{50k\Omega} = 12\mu A$$

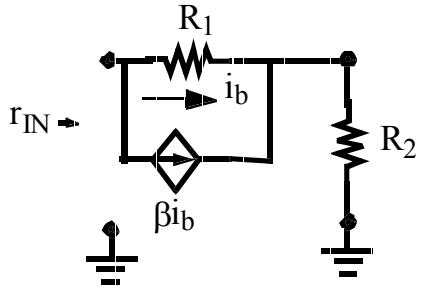
b) (12 Points) Find $v_{IN}$ when $v_{OUT}$ is 1.5V.

$$i_C = \beta i_b = \frac{(V_{DD} - V_{OUT})}{R_U} = \frac{(2.5V - 1.5V)}{1k\Omega} = 1mA$$

$$i_b = \frac{i_C}{\beta} = \frac{1mA}{100} = 10\mu A$$

$$V_{IN} = i_b R_{IN} + 0.7V + 0.7V = 10\mu A \cdot 50k\Omega + 1.4V = 1.9V$$

c) (14 Points) Find the input resistance for the circuit shown.




$$I_{TEST} = i_b + \beta i_b \qquad \Rightarrow i_b = \frac{I_{TEST}}{\beta + 1}$$

$$V_{TEST} = R_1 i_b + (\beta + 1) R_2 i_b$$

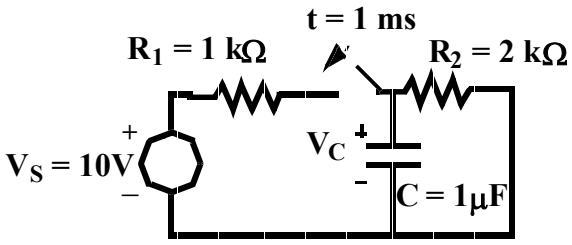
$$r_{IN} = \frac{V_{TEST}}{I_{TEST}} = \frac{R_1 i_b + (\beta + 1) R_2 i_b}{(\beta + 1) i_b} = \frac{R_1}{(\beta + 1)} + R_2$$

d) (6 Points) The input resistance in part c) above depends on $R_1$ and $R_2$. Does this circuit magnify, demagnify or not affect the contribution $R_1$?. Repeat for $R_2$ and briefly explain why the effects occur.

$R_1$ is demagnified by (β+1) as much of the current flows in parallel around it.
$R_2$ is unchanged (because it is in series and all currents flow through it.

## III (40 Points) Transients and Op-Amps

a) (9 Points) The switch in the circuit is closed at 1 ms. Just prior to closing the voltage on the capacitor is 3V. What was the voltage on the capacitor at t = 0?




$$V_C(t) = A + Be^{-t/\tau}$$

A = 0 because the capacitor can discharge fully.
T = $R_2C$ = 2kΩ 1μF = 2 ms

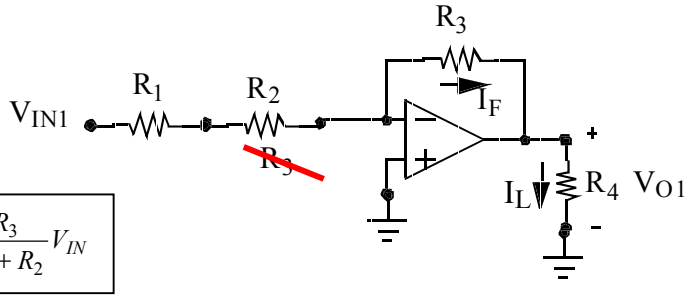
$$\Rightarrow V_C(t = 1ms) = Be^{-1ms/\tau}$$

$$B = V_C(t = 1ms)e^{1ms/\tau} = 3Ve^{1/2} = 4.95V$$

b) (6 Points) What is the time constant after the switch is closed?

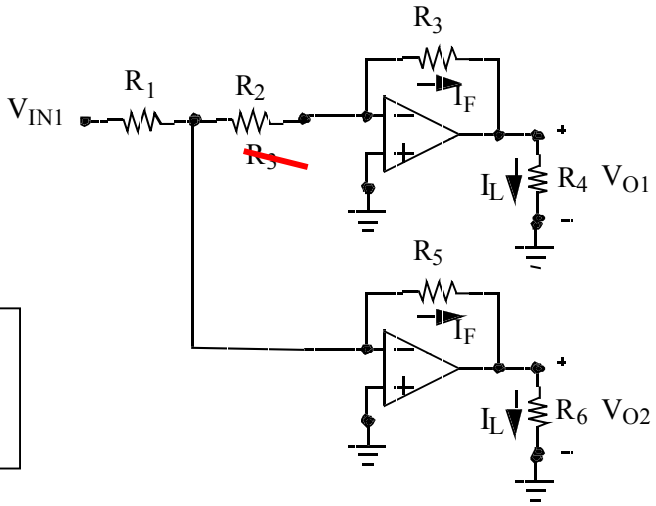
$$\tau = (R_1 \parallel R_2)C = 0.67k\Omega \cdot 1\mu F = 0.67ms$$

c) (10 Points) For the Op-Amp circuit to the right find $V_{OUT1}$ as a function of $V_{IN1}$.




$$\frac{V_{IN} - 0}{R_1 + R_2} + \frac{V_{OUT1}}{R_3} = 0 \Rightarrow V_{OUT1} = -\frac{R_3}{R_1 + R_2}V_{IN}$$

d) (15 Points) For the Op-Amp circuit to the right find $V_{OUT1}$ and $V_{OUT2}$ as a function of $V_{IN1}$. Be sure to show your fundamental assumptions. (Watch out this circuit may not be very useful.)

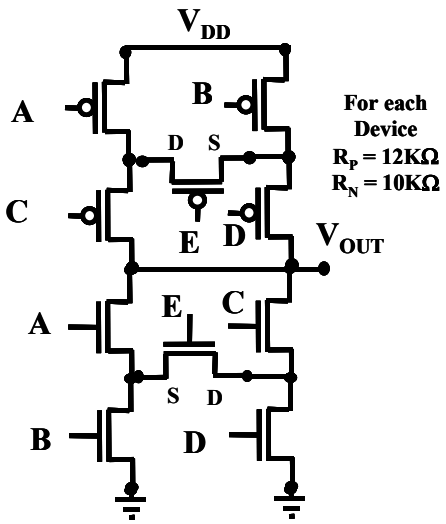



Note that both ends of $R_2$ are at the same (GND) potential so there is no current in $R_2$. As a result there is no current in $R_3$ and $V_{OUT1} = V^+ = 0$.

$$V_{OUT2} = -\frac{R_5}{R_1}V_{IN1}$$

## IV (38 Points) CMOS R, C and Carriers

a) (10 Points) Determine the worst-case resistance from the output to ground and give one example of inputs A-E for which this resistance will occur.




Worst case is to flow half way vertically in one arm, then move horizontally through E and then go the rest of the way vertically to ground in the other arm => $3R_N = 30k\Omega$. The inputs
A = 1, B = 0, C = 0, D = 1 and E = 1 do this.
Also
A = 0, B = 1, C = 1, D = 0 and E = 1 do this.

b) (15 Points) For the input state given to the right complete the table by specifying $V_{DD}$, GND or I (isolated) for each of the sources and drains in the circuit. For the vertical devices the NMOS source is toward the GND and the PMOS source is toward VDD. The horizontal devices are marked.

Input State: A = 0, B = 1, C = 1, D = 0, E = 0

| | A | B | C | D | E |
|---|---|---|---|---|---|
| **PMOS Source** | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ |
| **PMOS Drain** | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ |
| **NMOS Drain** | $V_{DD}$ | GND | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ |
| **NMOS Source** | GND | GND | $V_{DD}$ | GND | GND |

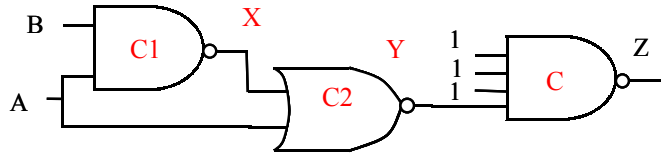
c) (13 Points) A 10 μm wide by 1 μm long NMOS transistor has carriers with a mobility of 200 $cm^2$/V-s and has a current of 10 μA when $V_{DS} = 0.1V$. Find the velocity of the carriers and the number of carriers per unit area under the gate. Hint: This problem requires only one very basic physical relationship and then some systematic reasoning. Several additional physical relationships have been added to the formula sheet to help you.

$$velocity = \mu E = \mu \frac{V}{L} = 200 cm^2/(Vs) \cdot \frac{0.1V}{10^{-4}} = 2 \cdot 10^5 cm/s$$

N is density/$cm^3$ and when multiplied by the thickness gives the density per unit area in the plan view.

## V (42 Points) CMOS Systems

a) (10 Points) Find the output logic levels of **X**, **Y**, and **Z** for the previous inputs when they have been applied for a long time and after the current inputs have been applied for a long time.

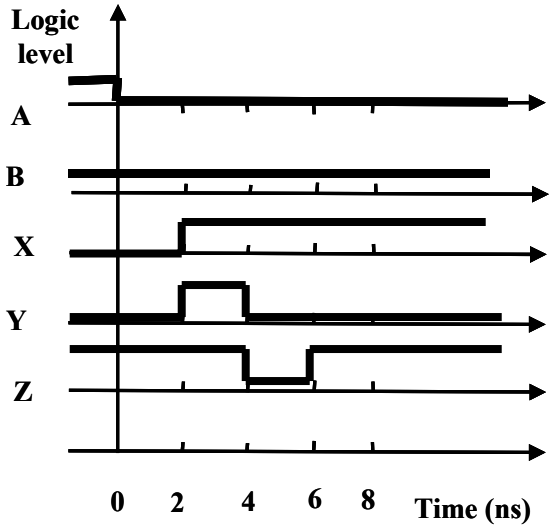



**Previous A = 1, B = 1, X = 0 , Y = 0 , Z = 1**

.

**Current A = 0, B = 1, X = 1 , Y = 0 , Z = 1**

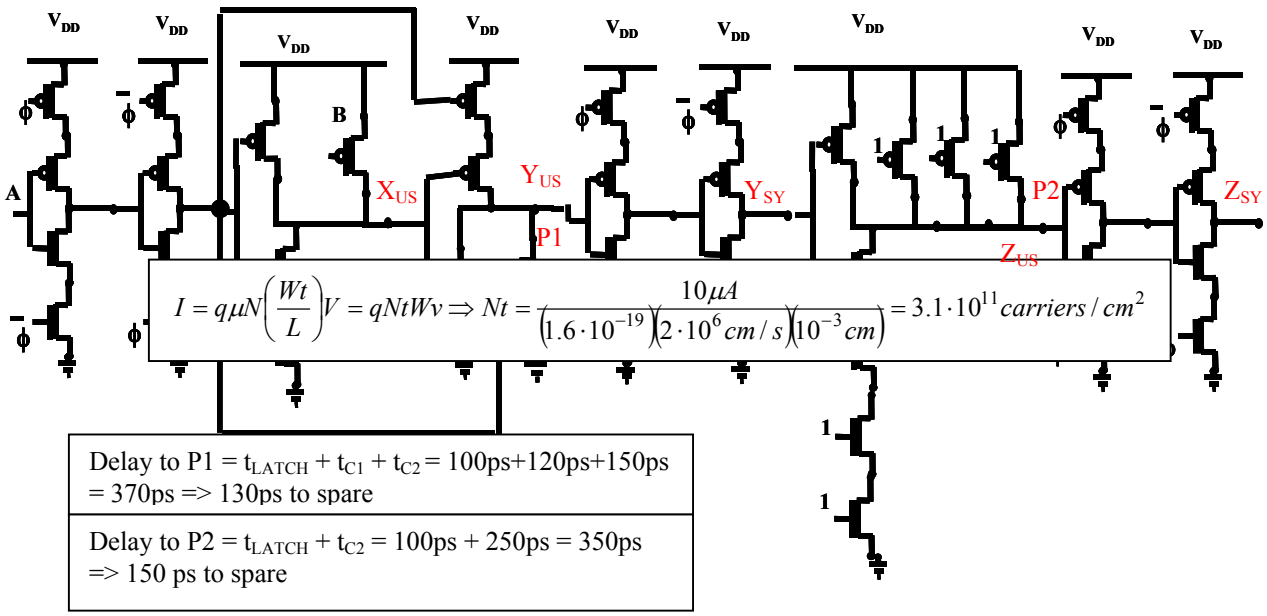
b) (15 Points) Assuming each gate transition takes 2 ns, complete the timing diagram using the changes in the inputs given in the timing diagram.




The same logic function is implemented with latches as shown below. Each stage of the latch takes 100 ps. Circuits C1, C2 and C3 take 120ps, 150 ps and 250 ps respectively. The clock is high for 500 ps and low for 200 ps. Assume the previous logic state has been applied for many clock cycles at the labeled inputs and just before the clock goes low-high the input A on the left side of the circuit goes high-low.

c) (6 Points) Label all nodes with occurrences of signals **X**, **Y** and **Z** in the circuit below and indicate which of these nodes are **unsynchronized** (subject to additional data dependent delays in combinatorial logic) and which are **synchronized** (pass the correct and final value within a short constant delay) with the low-high transition of the clock.

d) (11 Points). Label as P1 and P2 the two critical points in the interior of this circuit where the final value must arrive before the clock high-low transition occurs. Determine the excess time that the clock is high, by finding the propagation delay to **both** of these two critical points and comparing them to the 500 ps high.




$$I = q\mu N\left(\frac{Wt}{L}\right)V = qNtWv \Rightarrow Nt = \frac{10\mu A}{(1.6\cdot10^{-19})(2\cdot10^{6}\,cm/s)(10^{-3}\,cm)} = 3.1\cdot10^{11}\,carriers/cm^{2}$$

| |
|---|
| Delay to P1 = $t_{LATCH} + t_{C1} + t_{C2}$ = 100ps+120ps+150ps = 370ps => 130ps to spare |
| Delay to P2 = $t_{LATCH} + t_{C2}$ = 100ps + 250ps = 350ps => 150 ps to spare |