Equations for the Final Exam

Silicon Resistance

$$R = \rho L/A = (1/q\,\mu N)\, L/W = (L/W)/\mu(qNt)$$

$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS} - V_T)\cdot V_{OUT-SAT-n}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{(8.85x10^{-14}\,F/cm)(3.9)}{6x10^{-7}\,cm} = 5.75x10^{-7}\,F/cm^2$$

Device

	V_T(V)	$V_{OUT-SAT}$(V)	k' (μA/V²)
NMOS	0.43	0.63	100
PMOS	0.4	1	25

$$I_{OUT-SAT-n} = k_n'\left(\frac{W}{L}\right)_n (V_{IN} - V_{Tn})V_{OUT-SAT-n}$$

$$I_{OUT-SAT-p} = k_p'\left(\frac{W}{L}\right)_p (V_{DD} - V_{IN} - |V_{Tp}|)V_{OUT-SAT-p}$$

Device Circuit Model

$$R_D = \frac{V_{DD}}{2\cdot(0.69)I_{OUT-SAT-D}} \approx \frac{3}{4}\frac{V_{DD}}{I_{OUT-SAT-D}}$$

Power

$$P_{SHORT-CIRCUIT} = (P_A)\, I_{SHORT-CIRCUIT}\, V_{DD}\, \tau_{30-70}\, f_{CLOCK}$$

$$P_{DYNAMIC} = (1/2)\,(P_A)\, C\, V_{DD}^{\,2}\, f_{CLOCK}$$

Where P_A is the probability of one way switching activity per clock cycle