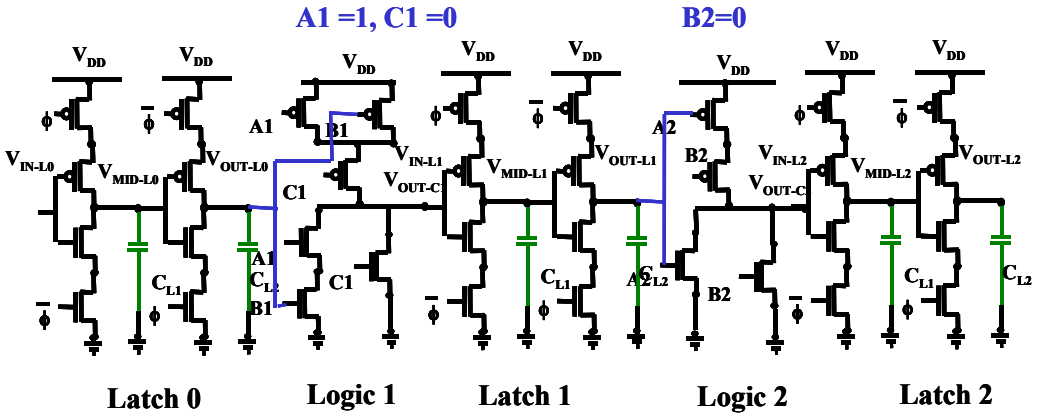
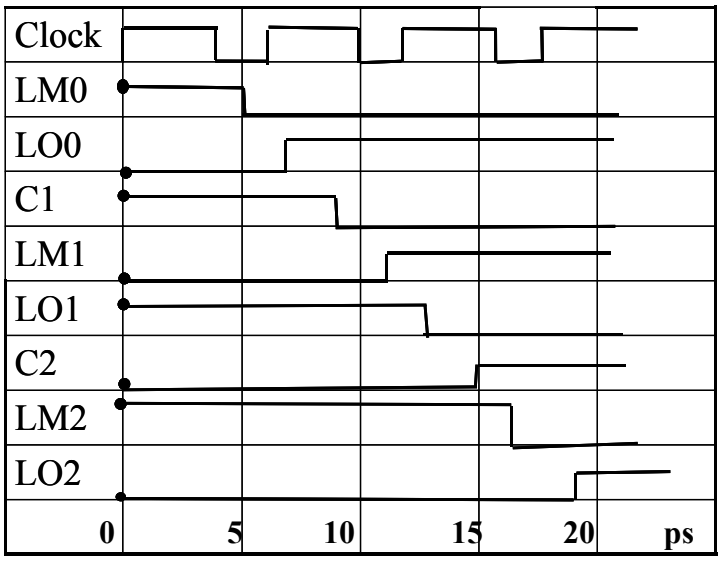
Answer Review Problems:



1) System Operation: Assume the clock has a 400 ps high followed by a 200 ps low. Also assume that the input to latch 0 has been low for many clock cycles. Also assume that a latch transition takes 100 ps and that the logic transition for ci5rcuit 1 is 200ps and for circuit 2 is 200 ps. Make a timing diagram for the circuit. That is, first sketch the clock for several cycles and then below it plot the response of each output in the circuit. Sketch the timing after input to latch 0 goes high.



2) Gate Operation: What is the delay for Logic 1 in the above circuit when A1 is no longer 1 and A1 and B1 are tied together?

Note 1: When devices are off there is an open circuit between source and drain. That is they are disconnected complete at the location of the gate.

Note 2: For the previous and current input states identify the voltage on each source and drain. This will usually identify each capacitance that changes voltage. Occasionally a node may have been isolated from Vdd or ground. In that case look at the problem statement for the previous history.

Capacitance on the NMOS node between B1 and A1 no longer switches. So

C_{EQ} = (3+3+3+3+1.5+0+0+1.5+3+1.5)(0.4fF)= 7.8fF

R_{UP} = 12kΩ+(12kΩ/2) = 18kΩ R_{DOWN} = 10kΩ + 10kΩ = 20kΩ

τ_{UP} = 0.69(6.8fF)(18kΩ) = 97ps τ_{DOWN} = 0.69(6.8fF)(20kΩ) = 108ps

Worst Case is now pull-down