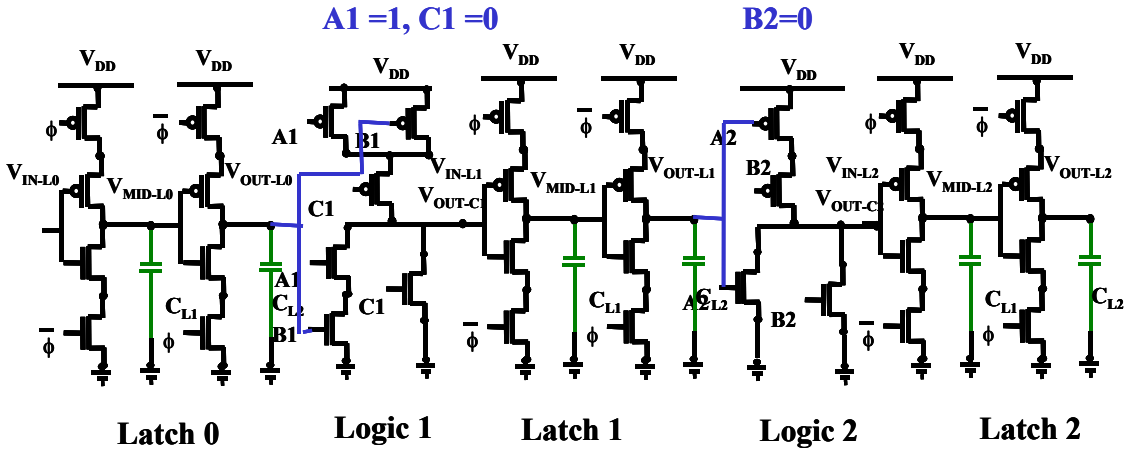
# Clarification: Latches on Final

## Coverage and Skills:

1) **Latch Big Picture: How two clocks and a latch circuit operate together to synchronize the flow of signals from one combinatorial logic gate to another even though the propagation delay of each of the combinatorial logic circuits is different.**
2) **System View: Given a set of input signals and clocks versus time and list of delays for latches and logic find how outputs behave versus time.**
3) **Data Dependent Logic Gate Propagation Delay: For a single combinatorial logic output node, find the delay for a given set of previous inputs to current inputs by finding the capacitors that change voltage, lumping them as an equivalent capacitance on the output node, and finding the net resistances of devices in series and parallel that allow current to flow to the output node.**
4) **Latch Propagation Delay: EE 42 convention that a latch has the source and drain capacitance load that is the same as that for an inverter.**
5) **Cascade: Apply delays for each stage to determine composite delay.**
6) **Fan-Out: Recognize Fan-Out and adjust the equivalent capacitance on the output node accordingly.**

## Review Problems: (Answer to appear on Sunday Evening 12/9/01)




1) **System Operation: Assume the clock has a 400 ps high followed by a 200 ps low. Also assume that the input to latch 0 has been low for many clock cycles. Also assume that a latch transition takes 100 ps and that the logic transition for ci5rcuit 1 is 200ps and for circuit 2 is 200 ps. Make a timing diagram for the circuit. That is, first sketch the clock for several cycles and then below it plot the response of each output in the circuit.**
2) **Gate Operation: What is the delay for Logic 1 in the above circuit when A1 is no longer 1 and A1 and B1 are tied together?**

**Homework Review List:**

**5.4 RC; 7.4 Op-Amp; 8.4 Dependent Source; 9.3 Load line; 10.2 Cascade**
**10.3 RC and dependent source gain; 10.5 CMOS; 11.4 Large Signal Diode**
**11.5 Perfect rectified Diode; 12.2 Large Signal Bipolar; 12.3 Resistance of silicon**
**13.4 CMOS power; 13.5 (see above)**